INSTRUCTION MANUAL

MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM

September, 1987 IM No. 597-0036

BROADCAST ELECTRONICS, INC.

IMPORTANT INFORMATION

EQUIPMENT LOST OR DAMAGED IN TRANSIT

When delivering the equipment to you, the truck driver or carrier's agent will present a receipt for your signature. Do not sign it until you have (a) inspected the containers for visible signs of damage and (b) counted the containers and compared with the amount shown on the shipping papers. If a shortage or evidence of damage is noted, insist that notation to that effect be made on the shipping papers before you sign them.

Further, after receiving the equipment, unpack it and inspect thoroughly for concealed damage. If concealed damage is discovered, immediately notify the carrier, confirming the notification in writing, and secure an inspection report. This item should be unpacked and inspected for damage WITHIN 15 DAYS after receipt. Claims for loss or damage will not be honored without proper notification of inspection by the carrier.

TECHNICAL ASSISTANCE AND REPAIR SERVICE

Technical assistance is available from Broadcast Electronics by letter or prepaid telephone or telegram. Equipment requiring repair or overhaul should be sent by common carrier, prepaid, insured and well protected. Do not mail equipment. We can assume no liability for inbound damage, and necessary repairs become the obligation of the shipper. Prior arrangement is necessary. Contact Customer Service Department for a Return Authorization.

FOR TECHNICAL ASSISTANCE
Phone (217) 224-9600 Customer Service

WARRANTY ADJUSTMENT

Broadcast Electronics, Inc. warranty is included in the Terms and Conditions of Sale. In the event of a warranty claim, replacement or repair parts will be supplied F.O.B. factory. At the discretion of Broadcast Electronics, the customer may be required to return the defective part or equipment to Broadcast Electronics, Inc. F.O.B. Quincy, Illinois. Warranty replacements of defective merchandise will be billed to your account. This billing will be cleared by a credit issued upon return of the defective item.

RETURN, REPAIR AND EXCHANGES

Do not return any merchandise without our written approval and Return Authorization. We will provide special shipping instructions and a code number that will assure proper handling and prompt issuance of credit. Please furnish complete details as to circumstances and reasons when requesting return of merchandise. All returned merchandise must be sent freight prepaid and properly insured by the customer.

REPLACEMENT PARTS

Replacement and Warranty Parts may be ordered from the address below. Be sure to include equipment model and serial number and part description and part number.

Broadcast Electronics, Inc.
4100 N. 24th St., P.O. Box 3606
Quincy, Illinois 62305
Tel: (217) 224-9600
Telex: 25-0142
Cable: BROADCAST

PROPRIETARY NOTICE

MODIFICATIONS

Broadcast Electronics, Inc. reserves the right to modify the design and specifications of the equipment in this manual without notice. Any modifications shall not adversely affect performance of the equipment so modified.

TECHNICAL MANUAL

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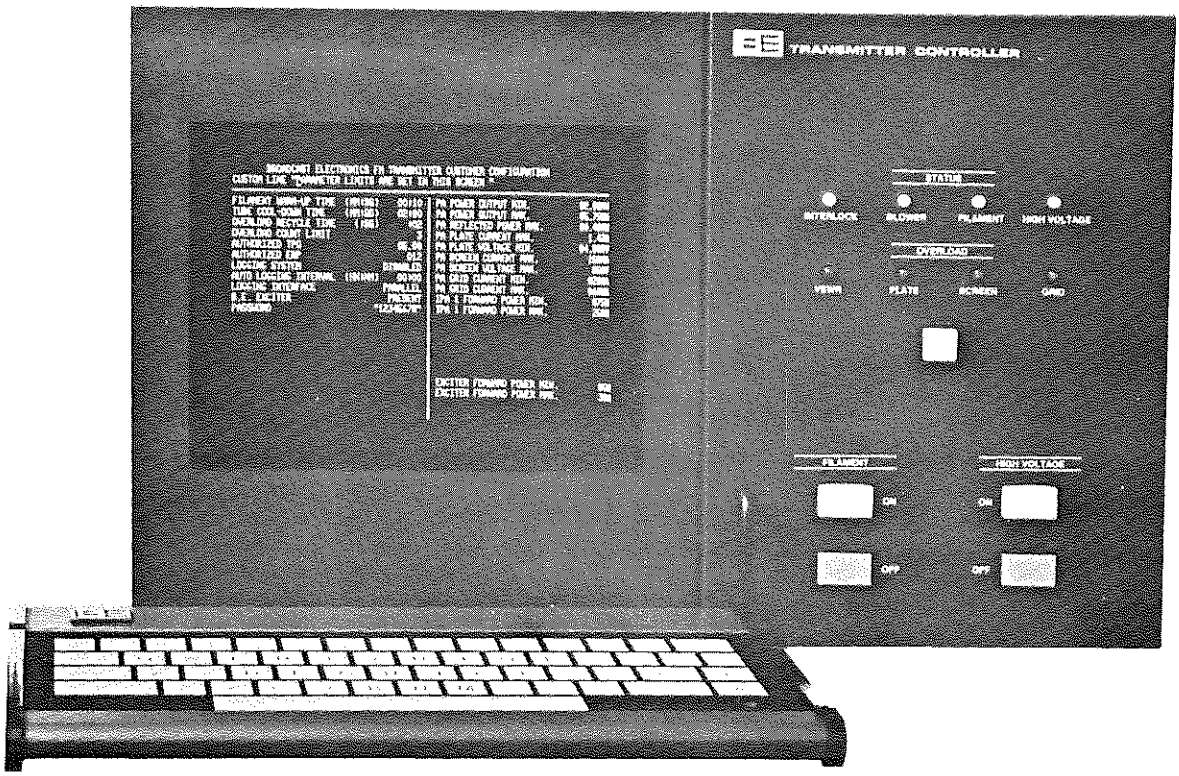
MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM

OPTION



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PART NUMBER	DESCRIPTION
909-0091-001	OPTIONAL MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM, FACTORY INSTALLATION, FM-30A TRANSMITTER.
909-0091-002	OPTIONAL MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM, FACTORY INSTALLATION, FM-3.5A TRANSMITTER.

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PART NUMBER	DESCRIPTION
909-0091-003	OPTIONAL MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM, FACTORY INSTALLATION, FM-5A TRANSMITTER.
909-0091-004	OPTIONAL MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM, FACTORY INSTALLATION, FM-1.5A TRANSMITTER.
909-0091-005	OPTIONAL MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM, FACTORY INSTALLATION, FM-10A TRANSMITTER.
909-0091-006	OPTIONAL MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM, FACTORY INSTALLATION, FM-35A TRANSMITTER.

FIELD INSTALLATION KITS

PART NUMBER	DESCRIPTION
979-0091-020	OPTIONAL MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM, FIELD INSTALLATION KIT, FM-1.5A TRANSMITTER.
979-0091-030	OPTIONAL MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM. FIELD INSTALLATION KIT, FM-3.5A TRANSMITTER.
979-0091-040	OPTIONAL MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM. FIELD INSTALLATION KIT, FM-5A TRANSMITTER.
979-0091-050	OPTIONAL MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM, FIELD INSTALLATION KIT, FM-30A TRANSMITTER.
979-0091-060	OPTIONAL MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM. FIELD INSTALLATION KIT, FM-10A TRANSMITTER.
979-0091-070	OPTIONAL MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM, FIELD INSTALLATION KIT, FM-35A TRANSMITTER.

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SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. Information presented by this section provides a general description of the Broadcast Electronics Microprocessor Video Diagnostic System and lists equipment specifications.

1-3. EQUIPMENT DESCRIPTION.

1-4. The Microprocessor Video Diagnostic System (MVDS) is a microprocessor based video display system which continuously monitors and displays all major transmitter parameters. The system contains five plug-in circuit boards, a power supply, a filter circuit board, a video monitor, and a system keyboard. All components are located within the controller cabinet and operate independently of the standard transmitter digital controller.

1-5. Transmitter parameter limits are selected by the operator and entered into the MVDS through the system keyboard. Transmitter limits and parameter status information are presented on three video display screens: the customer configuration screen, the normal display screen, and the bar-graph screen.

1-6. The customer configuration screen displays transmitter parameter limit information. Access to the screen is protected by an eight-digit password. Values are entered by the operator which establish the operating parameters for the transmitter. The values are stored in non-volatile memory for protection during a power failure.

1-7. The normal display screen displays the status of the transmitter parameters. Overloads and out-of-limit parameters are displayed in reverse video with a diagnosis of the transmitter condition. With this information, the operator is directed to a specific problem for troubleshooting.

1-8. The bar-graph screen displays selected transmitter parameters in a bar-graph and digital format. Out-of-limit parameters are displayed in reverse video for immediate recognition. The display can be used to tune the transmitter for overall efficiency or to check the transmitter operating parameters quickly.

1-9. A printed copy of the information presented on the normal display screen may be obtained through the MVDS logging system. Transmitter logs may be requested at the keyboard by the operator or provided automatically by the MVDS. A parallel and a serial port are provided for log printers. Logs may be transmitted through a modem or connected to an SCA generator for remote reception.

1-10. The microprocessor within the MVDS provides the transmitter with an additional independent and redundant controller. When the transmitter is operated with the microprocessor, most transmitter control operations as well as the diagnostic and display functions are performed by the MVDS. If the microprocessor is disabled, control will be automatically returned to the transmitter digital controller.

1-11. EQUIPMENT SPECIFICATIONS.

1-12. Refer to Table 1-1 for the system characteristics or Table 1-2 for physical characteristics of the Microprocessor Video Diagnostics System.

TABLE 1-1. SYSTEM CHARACTERISTICS
(Sheet 1 of 2)

PARAMETER	DESCRIPTION
POWER SUPPLY	Power One model HCCAA-60W-A. Completely independent of transmitter controller.
NON-VOLATILE MEMORY	2048 bytes. Storage of customer configuration screen data.
BATTERY SUPPORTED RANDOM ACCESS MEMORY	50 bytes. Storage of Clock and Overload data.
FILTERING	EMI filtering for all required communication signals to/from the logging devices.
COMMUNICATION PORTS	One parallel port. Three serial ports with selectable baud rates.
EXTERNAL VIDEO CONNECTION AND DISPLAY	One external video connection located on the rear panel of the controller cabinet. The Monitor can be extended a maximum of 1000 feet using RG59U cable terminated into 75 Ohms.

TABLE 1-1. SYSTEM CHARACTERISTICS
(Sheet 2 of 2)

PARAMETER	DESCRIPTION
MVDS DISPLAY ACCURACY:	
PLATE VOLTAGE	Within 0.5% of full scale.
PLATE CURRENT	Within 1.4% of full scale.
FORWARD POWER	Within 1.0% of full scale of calibrated power meter.

TABLE 1-2. PHYSICAL CHARACTERISTICS

PARAMETER	DESCRIPTION
AMBIENT TEMPERATURE RANGE	+14F to 122F (-10C to +50C).
MAXIMUM ALTITUDE:	
50 Hz Models	Ø to 7500 feet above sea level (Ø to 2286 meters).
60 Hz Models	Ø to 10,000 feet above sea level (Ø to 3048 meters).
MAXIMUM HUMIDITY	95%, Non-Condensing.
DIMENSIONS:	
WIDTH	19 Inches (48.26 cm).
HEIGHT	12.2 Inches (30.99 cm).
DEPTH	18.6 Inches (47.24 cm).
WEIGHT:	
MVDS OPTION	33 Pounds (14.9 kg).
MVDS OPTION WITH CONTROLLER	54 Pounds (24.3 kg).
COOLING AIR REQUIREMENTS	30 Cubic Feet per minute (0.85 m^3/min).

SECTION II
INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information required for the installation of the Broadcast Electronics Microprocessor Video Diagnostics System (MVDS).

2-3. UNPACKING.

2-4. The equipment becomes the property of the customer when the equipment is delivered to the carrier. Carefully unpack the monitor, keyboard, and the MVDS circuit boards. Perform a visual inspection to determine that no apparent damage has been incurred during shipment. All shipping materials should be retained until it is determined that the unit has not been damaged. Claims for damaged equipment must be promptly filed with the carrier or the carrier may not accept the claim.

2-5. The contents of the shipment should be as indicated on the packing list. If the contents are incomplete, or if the unit is damaged electrically or mechanically, notify both the carrier and Broadcast Electronics, Inc.

2-6. INSTALLATION.

NOTE IN THE FOLLOWING PROCEDURE, THE MVDS CLOCK BATTERY SWITCH ON THE INPUT/OUTPUT CIRCUIT BOARD MUST BE OPERATED TO ON.

NOTE

2-7. MVDS SWITCH AND JUMPER PROGRAMMING CHECK.

2-8. Each MVDS is programmed, operated, and tested at the factory prior to shipping. The following programming check assures the system circuit board jumpers have not become dislodged or the switches changed during shipment.

2-9. Refer to Figures 2-1 through 2-6 and ensure the system jumpers and switches are correctly positioned.

2-10. Refer to PART I, SECTION II of the applicable transmitter manual and ensure the controller circuit board jumpers are correctly positioned.

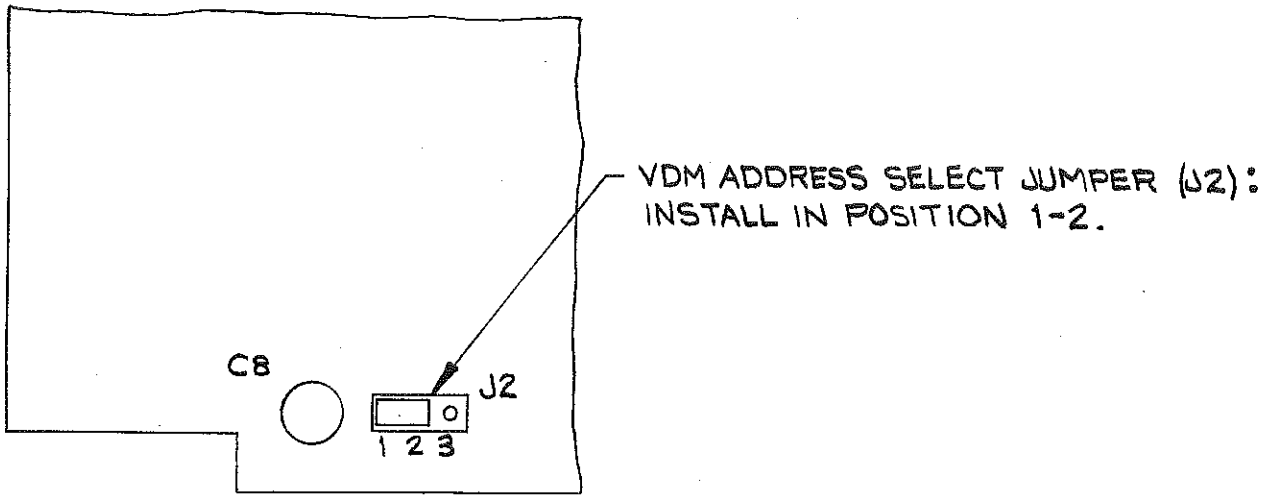

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FIGURE 2-1. VIDEO DISPLAY MODULE JUMPER PROGRAMMING

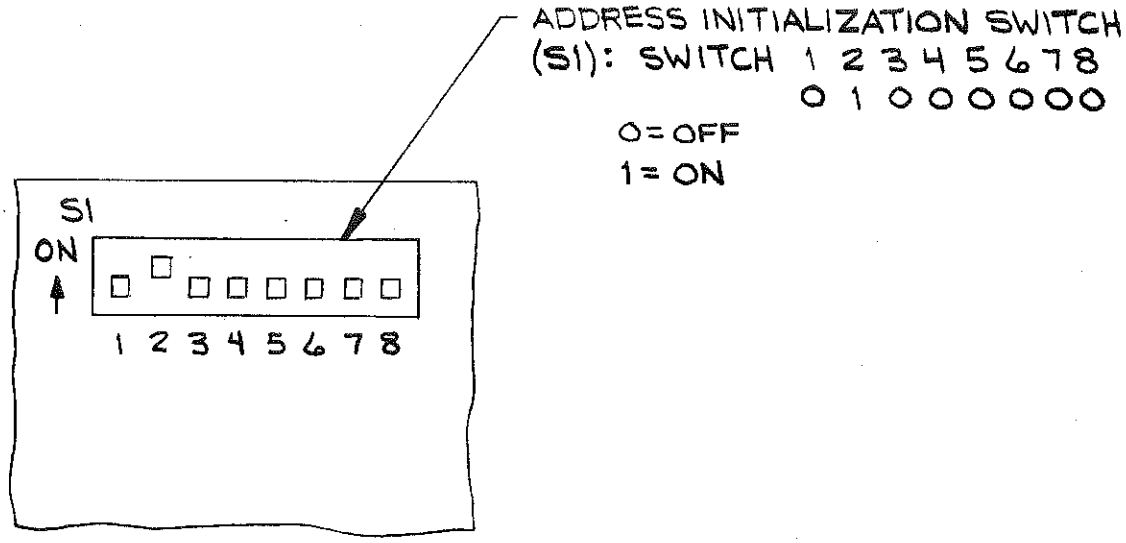

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FIGURE 2-2. CPU CIRCUIT BOARD SWITCH PROGRAMMING

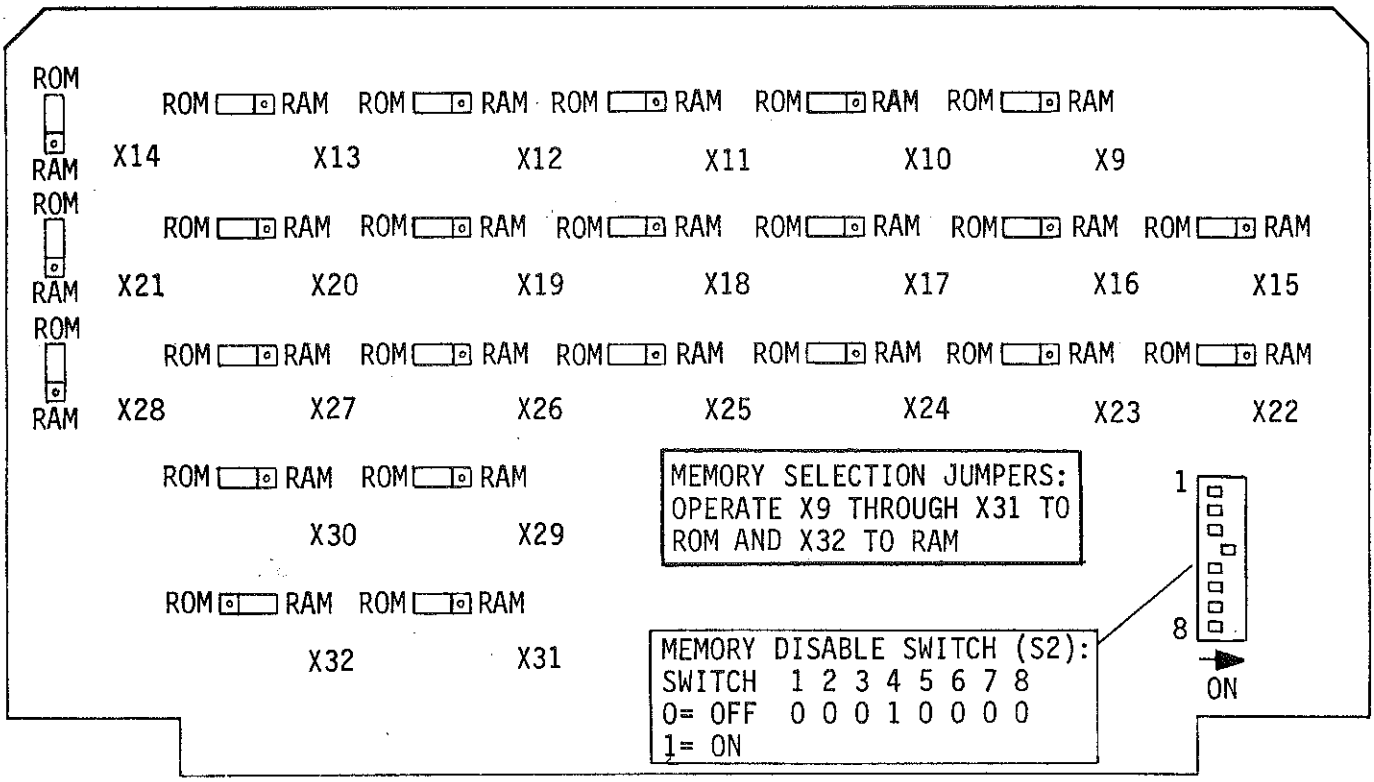

FIGURE 2-3. 64K MEMORY CIRCUIT BOARD JUMPER PROGRAMMING

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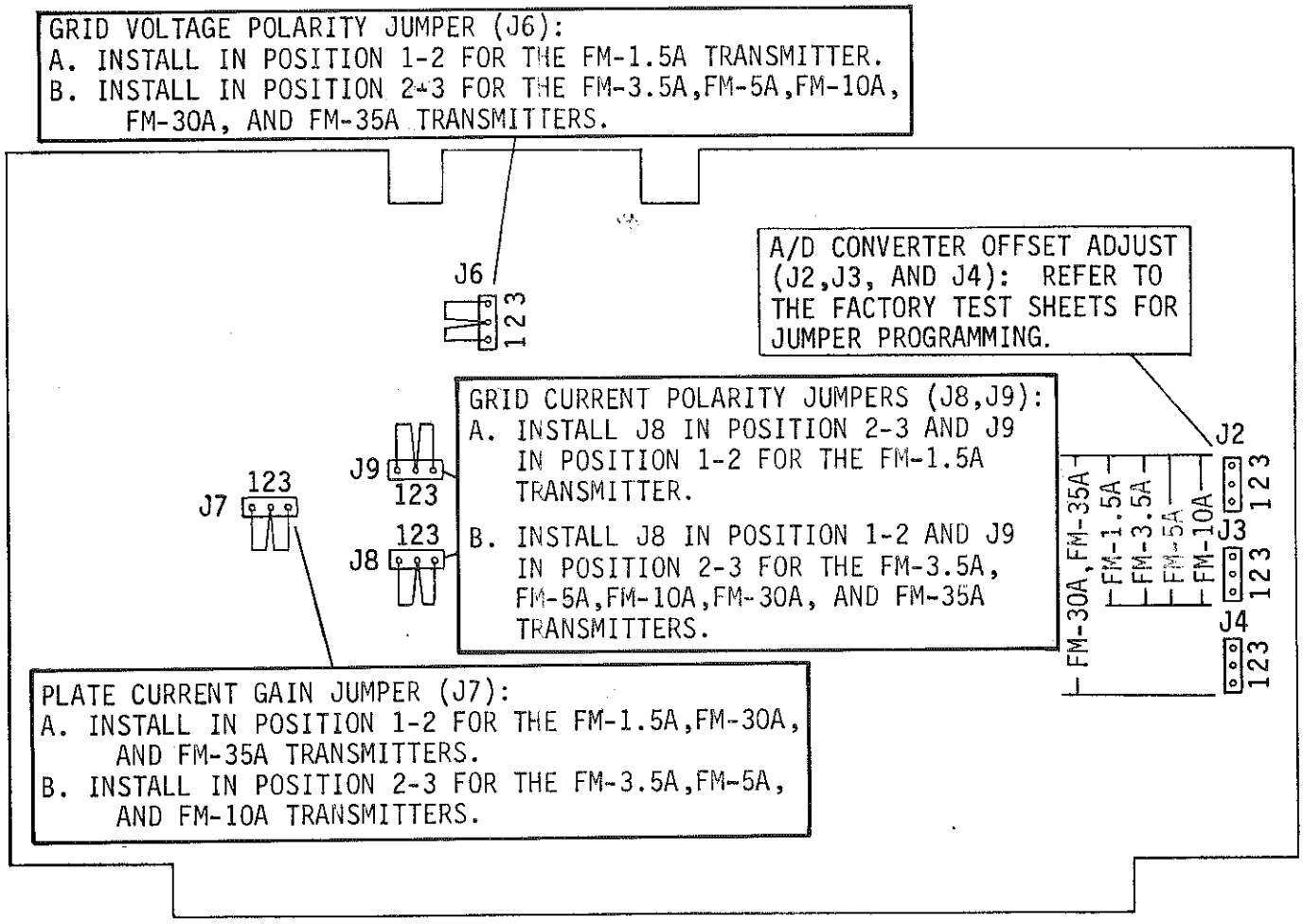

FIGURE 2-4. ANALOG/DIGITAL CIRCUIT BOARD JUMPER PROGRAMMING

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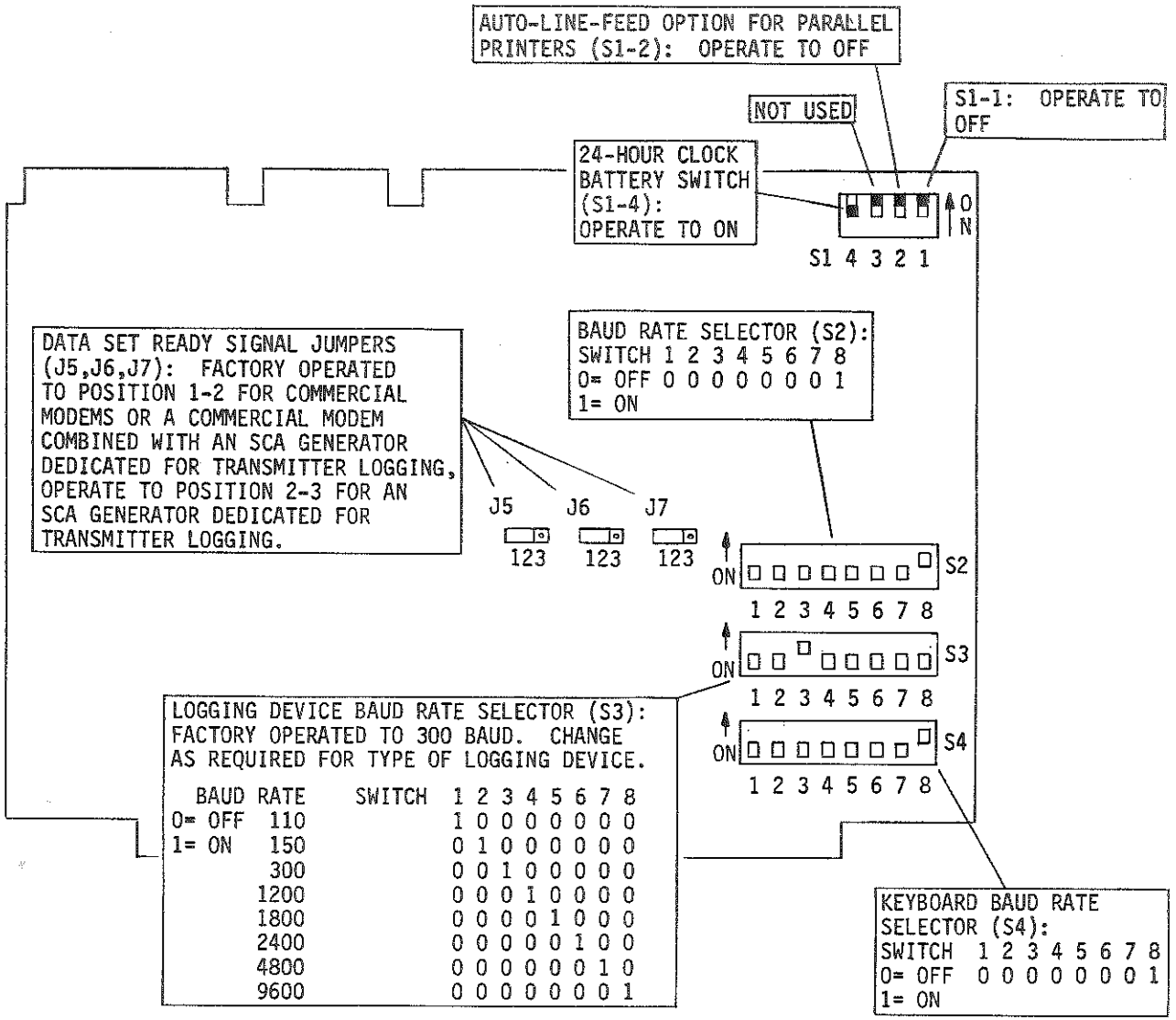

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FIGURE 2-5. INPUT/OUTPUT CIRCUIT BOARD JUMPER PROGRAMMING

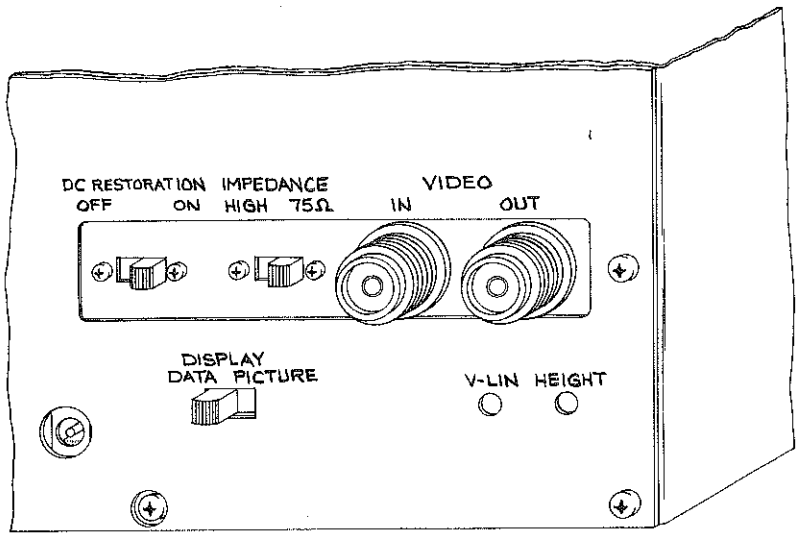

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FIGURE 2-6. MVDS VIDEO MONITOR SWITCH PROGRAMMING

2-11. VIDEO MONITOR AND CIRCUIT BOARD INSTALLATION.

WARNING ENSURE ALL TRANSMITTER PRIMARY POWER IS DISCONNECTED BEFORE PROCEEDING.

2-12. Ensure all transmitter primary power is disconnected before proceeding.

2-13. Refer to Figure 2-7 and install the MVDS video monitor as follows:

A. Open the transmitter controller cabinet doors and connect the video monitor ac line cord to the receptacle which is located at the top of the microprocessor power supply assembly.

B. Connect wire W10 to the monitor VIDEO IN jack.

C. Connect wire W6 to the monitor VIDEO OUT jack.

D. Slide the video monitor into the chassis opening and secure the two turnlock fasteners.

2-14. Refer to Figure 2-7 and install the MVDS circuit boards and connect the cables.

THE FOLLOWING CABLES ATTACH TO THE REAR OF THE MONITOR.

CABLE	RECEPTACLE
W10	VIDEO IN
W6	VIDEO OUT
MONITOR AC POWER	AC POWER RECEPTACLE W2

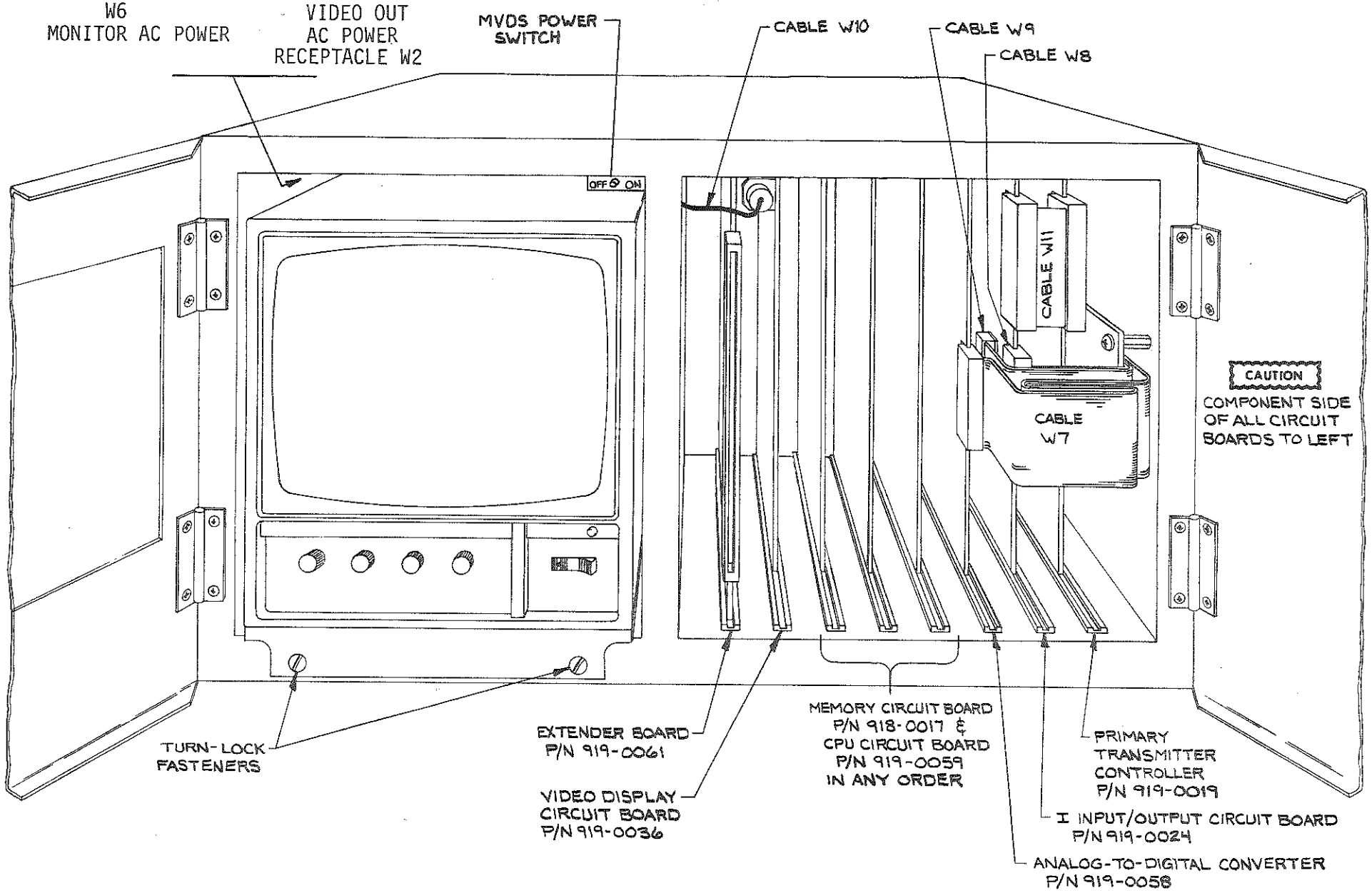

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FIGURE 2-7. CONTROLLER CABINET

2-15. COMMUNICATION EQUIPMENT CONNECTIONS.

2-16. KEYBOARD. The MVDS is provided with a system keyboard. Refer to Figure 2-9 and connect the keyboard cable to serial port J6 located on the rear-panel of the controller cabinet.

2-17. LOGGING DEVICES. A logging system is incorporated into the MVDS which allows the operator to obtain a printed copy of the transmitter parameters presented on the normal display screen. Different types of customer furnished logging devices may be connected to the MVDS. The following information and Figure 2-8 illustrate typical logging device applications. Cable information is provided in Section VII. The cables may be manufactured locally or purchased from Broadcast Electronics, Inc.

2-18. Local Serial Or Parallel Printer. Transmitter logs may be printed at the transmitter site through the use of an inexpensive home computer type parallel printer or a serial printer. Cable information is presented in drawing 949-0110 for the parallel printer and drawing 949-0113 for the serial printer.

2-19. Transmitting Log Information Through A Modem. Log information may be transmitted through a modem for remote reception by a serial printer or a personal computer. Two modems are required for logging operations: a transmitter site modem and a receiver site modem. Drawing 949-0114 provides cable information for the transmitter site modem.

2-20. In order for the modems to transmit and receive log information, the transmitter site modem and the studio modem must be operated with the following general characteristics.

TRANSMITTER SITE MODEM	STUDIO MODEM
1. Monitors and recognizes carrier detect.	1. The same baud rate as the transmitter site modem.
2. Auto-answer (Not required for dedicated line service).	
3. No interpretation of data as commands.	

2-21. Transmitting Log Information Through An SCA Generator. Log information may be transmitted through an SCA generator for remote reception. An SCA generator may be used alone or connected in parallel with a modem to provide an alternate logging method if the transmitter cycles off-the-air. Drawing 949-0111 provides cable information for the SCA generator and drawing 949-0112 provides information for the SCA generator combined with a modem.

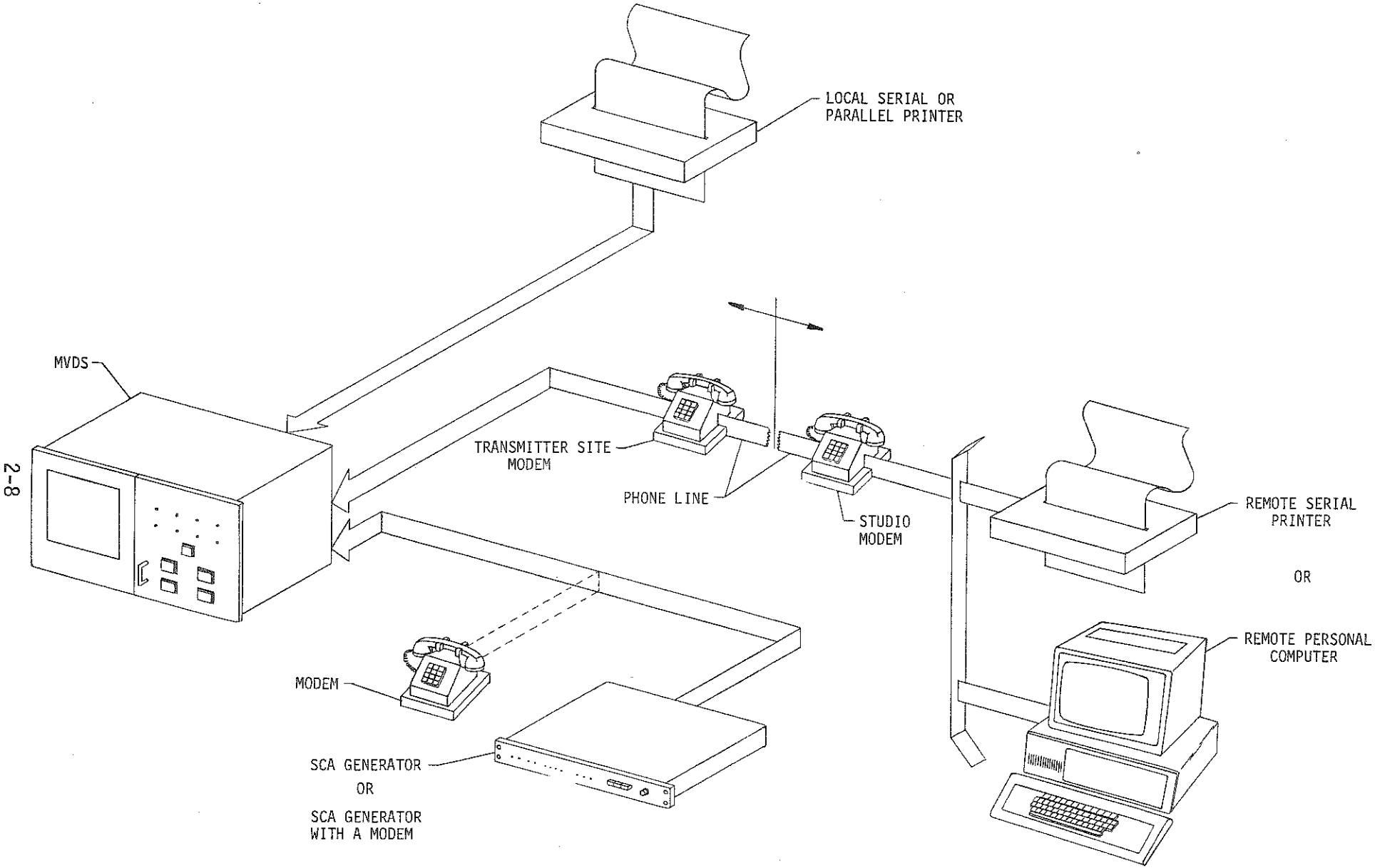

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FIGURE 2-8. TYPICAL LOGGING DEVICE APPLICATIONS

2-22. Logging Device Connections To The MVDS. Connections for the logging devices are provided on the rear panel of the controller cabinet. The following list describes each connector.

	CONNECTOR	TYPE OF PORT	SPECIFIC USE
J7	CENTRONICS	Parallel	Log Printer
J5	DCE2	Serial	Log Printer, Modem, SCA Generator, or SCA Generator with a Modem

2-23. Baud Rate Selection. Baud rate selection for devices connected to DCE2 is provided on the input/output circuit board. It is recommended that SCA logging be performed at 1200 baud, and modem logging be performed at 300 or 1200 baud, depending on the type of modem used. Refer to Figure 2-5 and ensure switch S3 is operated to the correct baud rate for the device.

2-24. CABLE ROUTING. Cables for the keyboard and the logging devices should be routed through the knock-out provided on the base plate of the transmitter. Inside the transmitter cabinet, route the cables as close to the cabinet frame as possible to avoid mechanical damage and connect the cable to the appropriate connector.

2-25. EXTERNAL VIDEO OUTPUT. The MVDS is provided with an external video output connector which is located on the rear-panel of the controller cabinet. Refer to Figure 2-9 and connect the device to the VIDEO OUT connector if external video is desired.

2-26. AC POWER CONNECTION.

WARNING ENSURE ALL PRIMARY POWER IS DISCONNECTED BEFORE PROCEEDING.

2-27. A transmitter controller which is equipped with an MVDS system is programmed for the proper power supply voltage when shipped from the factory. Refer to Figure 2-9 and remove the fuse from the rear-panel fuse-holder. Ensure the fuse is a slow-blow type rated at 2A for 220V operation.

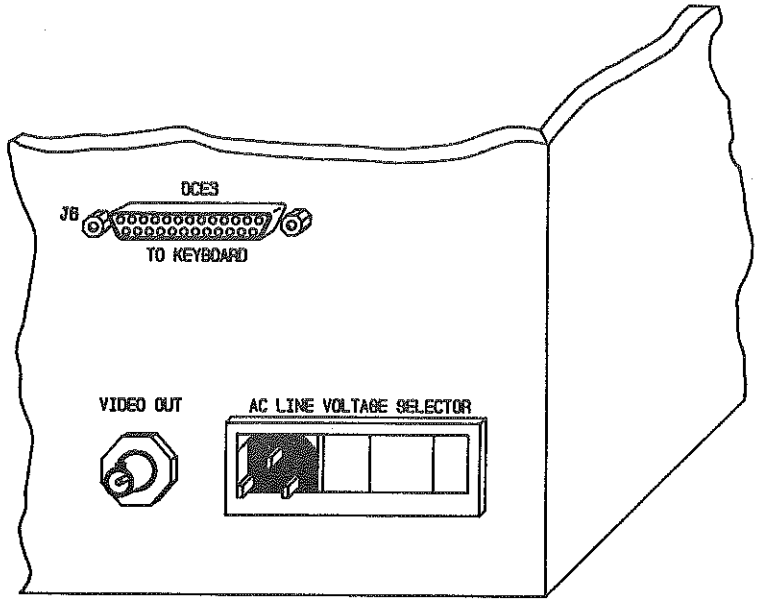

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FIGURE 2-9. REAR-PANEL OF CONTROLLER CABINET

SECTION III
OPERATION

3-1. INTRODUCTION.

3-2. This section provides initial entry and standard operating procedures for the Broadcast Electronics Microprocessor Video Diagnostics System.

3-3. INITIAL OPERATION.

3-4. KEYBOARD.

3-5. Initial operation begins with the operation of the keyboard which provides communication between the operator and the MVDS. Refer to Figure 3-1 and Table 3-1 and learn the basic keyboard commands and special key functions.

3-6. TURN-ON.

CAUTION — ENSURE THE TRANSMITTER IS OFF AND ALL CIRCUIT BREAKERS ARE OFF BEFORE PROCEEDING.

NOTE — ENSURE THE TRANSMITTER IS COMPLETELY INSTALLED AND OPERATING PROPERLY BEFORE PROCEEDING.

3-7. If the transmitter is on-the-air, operate the transmitter to OFF and operate all circuit breakers to OFF.

3-8. Operate the following circuit breakers to ON:

FM-1.5A	AC POWER	DRIVER
FM-3.5A/5A	AC POWER	BLOWER
FM-10A	PRIMARY	DRIVER
FM-30A	PRIMARY	DRIVER
FM-35A	PRIMARY	DRIVER

3-9. Operate the MVDS power switch (located above the monitor) to ON.

3-10. NORMAL DISPLAY SCREEN (Screen 1). With power applied, the normal display screen (screen 1) will appear on the monitor. Refer to Figure 3-2 and Table 3-2 for a description of the display.

3-11. Clock Set Procedure. To program the 24-hour clock, proceed as follows:

3-12. Before programming the 24-hour clock, depress the transmitter OVERLOAD reset switch to remove the POWER FAILURE warning.

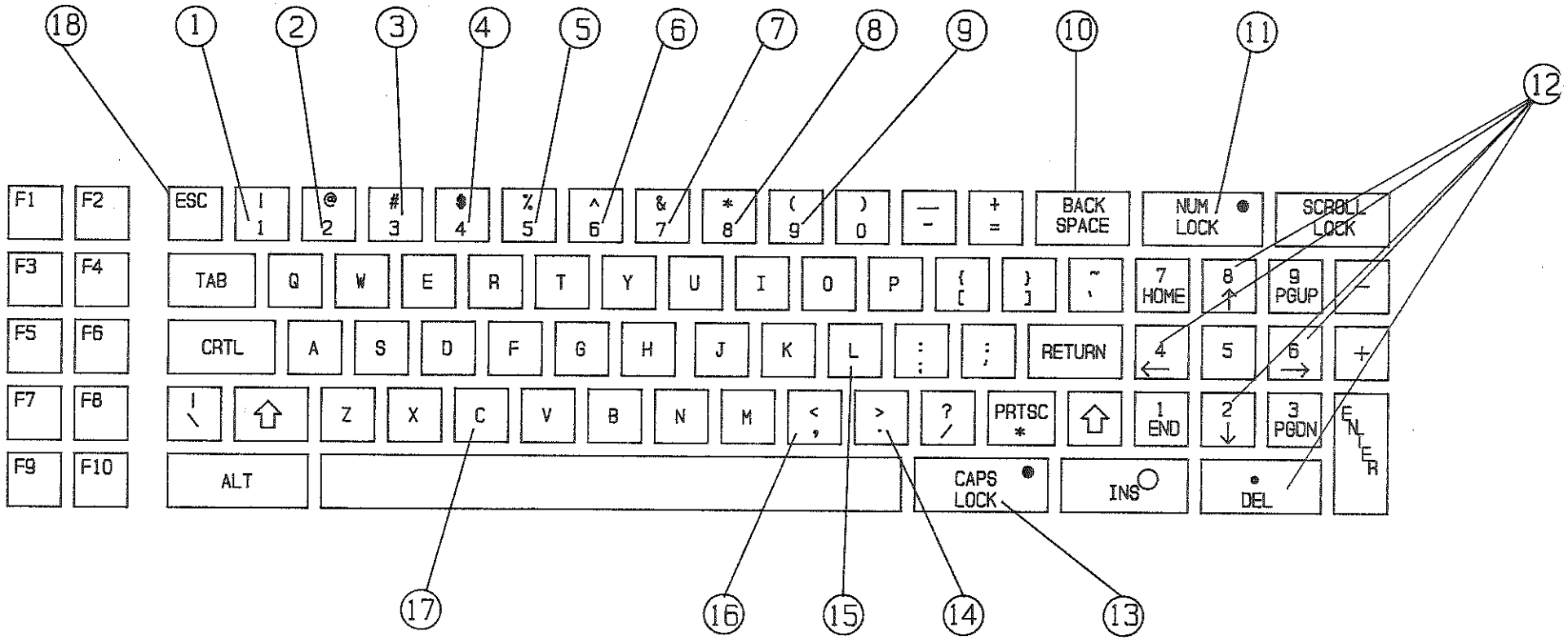

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FIGURE 3-1. KEYBOARD

TABLE 3-1. KEYBOARD COMMANDS

INDEX NUMBER	DESCRIPTION
1	Advances the day-of-the-week in the CLOCK SET mode.
2	Advances the month in the CLOCK SET mode and accesses the bar-graph screen (screen 2).
3	Advances the day in the CLOCK SET mode and accesses the customer configuration screen (screen 3).
4	Advances the year in the CLOCK SET mode.
5	Advances the hours in the CLOCK SET mode.
6	Advances the minutes in the CLOCK SET mode.
7	Advances the seconds in the CLOCK SET mode.
8	Toggles the 24-hour clock between military time (18:30:ØØ) and normal civilian time (06:30:ØØPM).
9	Starts and stops the 24-hour clock.
10	Cursor backspace.
11	Toggles the 2, 4, 6, 8, and DEL keys of the numeric keypad between numeric operation (LED illuminated) and cursor operation (LED extinguished).
12	Enters numeric data when the NUM LOCK LED is illuminated. When the NUM LOCK LED is extinguished, the keys perform cursor operations (left, right, up and down).
13	Provides upper case character entry.
14	Cursor advance (depress the ⇧ and >).
15	Requests a log of the normal display screen when operated during the normal or bar-graph display screen.
16	Cursor backspace (depress the ⇧ and <).
17	Accesses the CLOCK SET mode (CLOCK SET is only accessible from the normal display screen).
18	Terminates the CLOCK SET mode and accesses the normal display screen (screen 1).

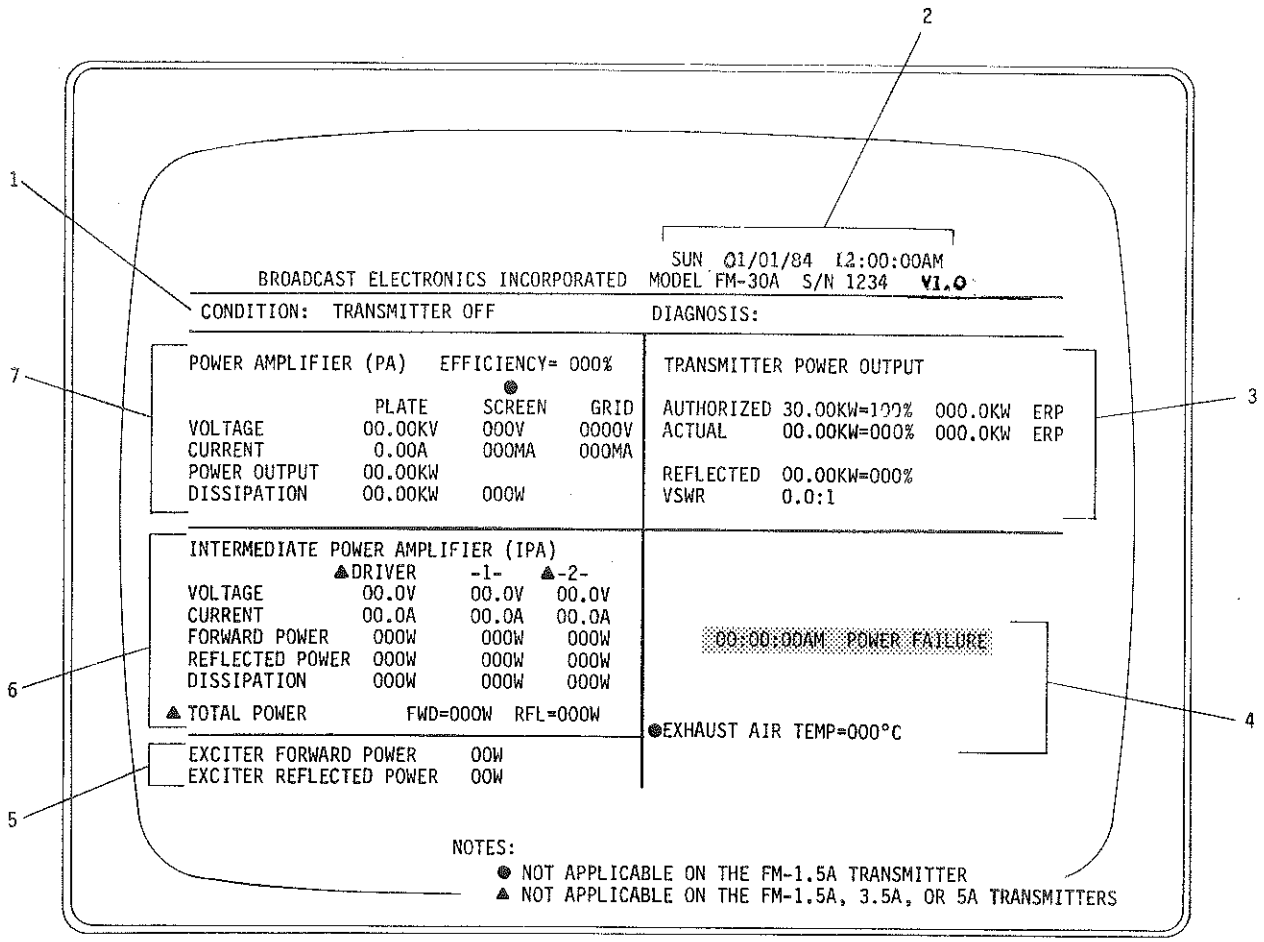

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FIGURE 3-2. NORMAL DISPLAY SCREEN (Screen 1)

3-13. Depress the CAPS LOCK key for upper case character entry. The CAPS LOCK indicator will illuminate.

3-14. Operate the NUM LOCK key to extinguish the NUM LOCK indicator.

3-15. Depress the C key (CLOCK SET will appear on the lower right-hand corner of the screen).

3-16. Depress the DELETE key (resets the 24-hour clock).

3-17. Depress key 1 until the correct day-of-the-week appears on the 24-hour clock.

3-18. Depress key 2 until the correct month appears on the 24-hour clock.

3-19. Depress key 3 until the correct day appears on the 24-hour clock.

TABLE 3-2. NORMAL DISPLAY SCREEN (SCREEN 1)

INDEX NUMBER	DESCRIPTION
1	Displays the present condition of the transmitter and the reason for the condition.
2	Displays the 24-hour clock which is programmed by the operator. The 24-hour clock will automatically change with daylight savings time and leap year.
3	Displays the status of the TRANSMITTER POWER OUTPUT parameters: ACTUAL ERP, REFLECTED power, and VSWR.
4	Displays all overload conditions in reverse video and the following transmitter and MVDS statuses. Transmitter: EXHAUST AIR TEMP.; APC ON; APC PRESET POWER; REMOTE CONTROL ON MVDS: LOG PRINTING; CLOCK SET; ENABLED (Log); MPU (microprocessor unit) CONTROL
5	Displays the status of the EXCITER FORWARD and REFLECTED POWER parameters.
6	Displays the status of the IPA VOLTAGE, CURRENT, FORWARD POWER, REFLECTED POWER, DISSIPATION, and TOTAL POWER parameters.
7	Displays the status of the PA PLATE, SCREEN, and GRID parameters.

3-20. Depress key 4 until the correct year appears on the 24-hour clock.

3-21. Depress key 5 until the correct hour appears on the 24-hour clock.

3-22. Depress key 6 until the correct minutes appear on the 24-hour clock.

3-23. Depress key 7 until the correct seconds appear on the 24-hour clock.

3-24. Depress key 8 to convert the 24-hour clock into military time (example 18:30:ØØ) or depress key 8 again for normal civilian time (example 06:30:ØØAM).

3-25. Depress key 9 to manually start (or stop) the 24-hour clock.

3-26. Depress the ESCAPE key (CLOCK SET will disappear from the display and the 24-hour clock will automatically start).

3-27. CUSTOMER CONFIGURATION SCREEN (Screen 3). The next step in initial operation is to access the customer configuration screen which is protected by an eight-digit password. Screen 3 allows the operator to enter maximum and minimum limits of transmitter parameters. The operator must enter limits which are within the factory-set safe operating levels for each model of transmitter. If a limit is entered which is above or below the safe operating level, the cursor will not advance to the next field of entry. To access screen 3, proceed as follows:

3-28. Depress key 3 (ENTER PASSWORD: " " will appear on the screen).

3-29. Enter 12345678 which is the factory default PASSWORD.

3-30. Screen 3 will appear on the monitor. Refer to Figure 3-3 and Table 3-3 for a description of the display.

3-31. Procedure. To program the customer configuration screen, proceed as follows:

3-32. Enter any desired message on the CUSTOM LINE (40 characters maximum).

3-33. Depress the $\overset{2}{\downarrow}$ key.

3-34. Enter the FILAMENT WARM-UP TIME. The factory operating limits are:

	Maximum	Minimum
FM-1.5A	59:59	03:ØØ
FM-3.5A/ 5A/10A/ 30A/35A	59:59	ØØ:10

TABLE 3-3. CUSTOMER CONFIGURATION SCREEN (Screen 3)

INDEX NUMBER	DESCRIPTION
1	An operator entered message which has a maximum length of 40 characters (example WBEI-FM 103.3 MHz) and no effect on transmitter parameters.
2	Operator minimum and maximum limits for transmitter parameters (values displayed on the screen are factory default limits). The operator entered limits must be within the factory-set safe operating levels or the cursor will not advance to the next field of entry.
3	An operator password which is eight-characters long. When entered into the MVDS, the operator password will replace the factory default password (12345678).
4	Type of communication used by the log interface (serial or parallel).
5	The length of time between log printouts (example ØØ:10 - a log will print every 10 minutes).
6	The indirect efficiency factor is an efficiency value which is calculated and entered at the factory and displayed on the PA section of screen 1 (if the indirect power measurement method is selected). The indirect efficiency factor must be updated as required to reflect the changes in transmitter efficiency.
7	The number of overloads the transmitter will accept before the transmitter will deenergize and must be manually reset.
8	The length of time the transmitter remains off-the-air after an overload to allow the condition that prompted the overload to dissipate.

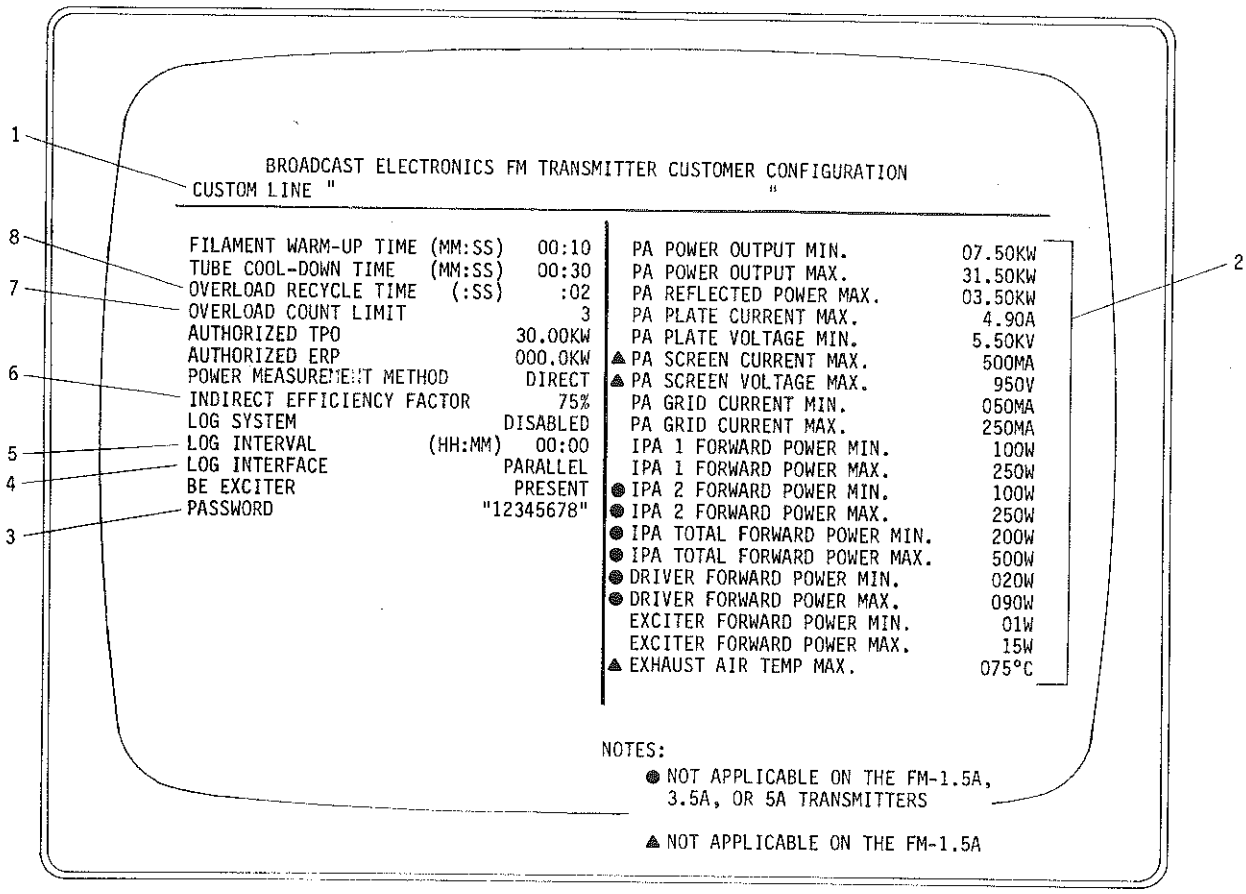

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FIGURE 3-3. CUSTOMER CONFIGURATION SCREEN (Screen 3)

3-35. Depress the 2↓ key.

3-36. Enter the TUBE COOL-DOWN TIME. The factory operating limits are:

	Maximum	Minimum
FM-1.5A	59:59	03:ØØ
FM-3.5A/ 5A/10A/ 30A/35A	59:59	ØØ:30

3-37. Depress the 2↓ key.

3-38. Enter the OVERLOAD RECYCLE TIME. The factory operating limits are:

	Maximum	Minimum
All Models	ØØ:59	ØØ:01

3-39. Depress the 2↓ key.

3-40. Enter the OVERLOAD COUNT LIMIT. The factory operating limits are:

	Maximum	Minimum
All Models	9	Ø

3-41. Depress the 2↓ key.

3-42. Enter the AUTHORIZED TPO (transmitter power output).

3-43. Depress the 2↓ key.

3-44. Enter the AUTHORIZED ERP.

3-45. Depress the 2↓ key.

3-46. Enter the POWER MEASUREMENT METHOD.

D= DIRECT
I= INDIRECT

3-47. Depress the 2↓ key.

3-48. The INDIRECT EFFICIENCY FACTOR is factory calculated and entered into the display during final testing. The indirect efficiency factor must be updated as required to reflect the changes in transmitter efficiency. If the DIRECT method was selected in the above step, the indirect efficiency factor has no effect on power output calculations and may be disregarded.

3-49. Depress the 2↓ key.

3-50. Enter the LOG SYSTEM status.

D= DISABLED
E= ENABLED

3-51. Depress the 2↓ key.

3-52. Enter the LOG INTERVAL. If no periodic logging is required, enter ØØ:ØØ.

3-53. Depress the 2↓ key.

3-54. Enter the type of LOG INTERFACE communication.

P= PARALLEL
S= SERIAL

3-55. Depress the 2↓ key.

3-56. Enter the correct response for BE EXCITER.

P= PRESENT
A= ABSENT

3-57. Depress the 2 ↓ key.

3-58. Enter the operator PASSWORD. The password must be eight characters long and can be any letter, number, or special character (characters above the number keys). This password replaces the factory default password.

3-59. If the customer password is forgotten in the future, contact the Broadcast Electronics Customer Service Department.

3-60. Depress the 2 ↓ key.

3-61. Enter the PA POWER OUTPUT MIN. The factory minimum limits are:

FM-1.5A	FM-3.5A	FM-5A	FM-10A	FM-30A	FM-35A
ØØ.45KW	01.35KW	02.ØØKW	04.00KW	07.50KW	07.50KW

3-62. Depress the 2 ↓ key.

3-63. Enter the PA POWER OUTPUT MAX. The factory maximum limits are:

FM-1.5A	FM-3.5A	FM-5A	FM-10A	FM-30A	FM-35A
01.75KW	04.ØØKW	05.75KW	11.50KW	31.ØØKW	36.75KW

3-64. Depress the 2 ↓ key.

3-65. Enter the PA REFLECTED POWER MAX. The factory maximum limits are:

FM-1.5A	FM-3.5A	FM-5A	FM-10A	FM-30A	FM-35A
ØØ.16KW	ØØ.35KW	ØØ.40KW	ØØ.80KW	03.ØØKW	03.00KW

3-66. Depress the 2 ↓ key.

3-67. Enter the PA PLATE CURRENT MAX. The factory maximum limits are:

FM-1.5A	FM-3.5A	FM-5A	FM-10A	FM-30A	FM-35A
Ø.80A	1.35A	1.42A	2.50A	4.90A	4.90A

3-68. Depress the 2 ↓ key.

3-69. Enter the PA PLATE VOLTAGE MIN. The factory minimum limits are:

FM-1.5A	FM-3.5A	FM-5A	FM-10A	FM-30A	FM-35A
02.20KV	03.90KV	04.80KV	05.00KV	05.50KV	05.50KV

3-70. Depress the 2↓ key.

3-71. Enter the PA SCREEN CURRENT MAX (not applicable on the FM-1.5A). The factory maximum limits are:

FM-3.5A	FM-5A	FM-10A	FM-30A	FM-35A
150mA	150mA	150mA	500mA	500mA

3-72. Depress the 2↓ key.

3-73. Enter the PA SCREEN VOLTAGE MAX (not applicable on the FM-1.5A). The factory maximum limits are:

FM-3.5A	FM-5A	FM-10A	FM-30A	FM-35A
750V	850V	900V	900V	900V

3-74. Depress the 2↓ key.

3-75. Enter the PA GRID CURRENT MIN. The factory minimum limits are:

FM-1.5A	FM-3.5A	FM-5A	FM-10A	FM-30A	FM-35A
ØØØmA	020mA	020mA	020mA	050mA	050mA

3-76. Depress the 2↓ key.

3-77. Enter the PA GRID CURRENT MAX. The factory maximum limits are:

FM-1.5A	FM-3.5A	FM-5A	FM-10A	FM-30A	FM-35A
175mA	060mA	060mA	100mA	200mA	200mA

3-78. Depress the 2↓ key.

3-79. Enter the IPA 1 FORWARD POWER MIN. The factory minimum limits are:

FM-1.5A	FM-3.5A	FM-5A	FM-10A	FM-30A	FM-35A
025W	075W	075W	075W	100W	100W

3-80. Depress the 2↓ key.

3-81. Enter the IPA 1 FORWARD POWER MAX. The factory maximum limits are:

FM-1.5A	FM-3.5A	FM-5A	FM-10A	FM-30A	FM-35A
100W	220W	250W	250W	280W	280W

3-82. Depress the 2↓ key.

3-83. Enter the IPA 2 FORWARD POWER MIN (FM-30A and FM-35A only). The factory minimum limit is:

FM-30A	FM-35A
100W	100W

3-84. Depress the 2↓ key.

3-85. Enter the IPA 2 FORWARD POWER MAX (FM-30A and FM-35A only). The factory minimum limit is:

FM-30A	FM-35A
280W	280W

3-86. Depress the 2↓ key.

3-87. Enter the IPA TOTAL FORWARD POWER MIN (FM-30A and FM-35A only). The factory minimum limit is:

FM-30A	FM-35A
160W	160W

3-88. Depress the 2↓ key.

3-89. Enter the IPA TOTAL FORWARD POWER MAX (FM-30A and FM-35A only). The factory maximum limit is:

FM-30A	FM-35A
448W	448W

3-90. Depress the 2↓ key.

3-91. Enter the DRIVER FORWARD POWER MIN (FM-30A and FM-35A only). The fac- tory minimum limit is:

FM-30A	FM-35A
020W	020W

3-92. Depress the 2↓ key.

3-93. Enter the DRIVER FORWARD POWER MAX (FM-30A and FM-35A only). The factory maximum limit is:

FM-30A	FM-35A
080W	080W

3-94. Depress the 2↓ key.

3-95. Enter the EXCITER FORWARD POWER MIN. The factory minimum limits are:

FM-1.5A	FM-3.5A	FM-5A	FM-10A	FM-30A	FM-35A
02W	05W	05W	05W	03W	03W

3-96. Depress the 2↓ key.

3-97. Enter the EXCITER FORWARD POWER MAX. The factory maximum limits are:

FM-1.5A	FM-3.5A	FM-5A	FM-10A	FM-30A	FM-35A
25W	25W	30W	40W	20W	20W

3-98. Depress the $\overset{2}{\downarrow}$ key.

3-99. Enter the EXHAUST AIR TEMP. MAX (FM-3.5A, FM-5A, FM-10A, FM-30A and FM-35A only). The factory maximum limits are:

FM-3.5A	FM-5A	FM-10A	FM-30A	FM-35A
75°C	75°C	75°C	95°C	95°C

3-100. TRANSMITTER OPERATION WITH MVDS.

3-101. After the customer configuration screen has been properly programmed, the last step is to operate the transmitter with the MVDS. The status of the transmitter parameters will be displayed on the normal display screen (screen 1) and the bar-graph screen (screen 2).

3-102. OPERATION OF THE NORMAL DISPLAY SCREEN.

3-103. Access the normal display screen by depressing the ESCAPE key (the normal display screen will appear on the monitor). The operator can access the normal display screen at any time by depressing the ESCAPE key.

3-104. Operate the transmitter at the normal RF power output. The normal display screen will display the status of the transmitter parameters. After the transmitter has cycled-on, a Transmitter On Log of the normal display screen will be printed by the MVDS (if the logging system has been enabled).

3-105. Observe the normal display screen values and the Transmitter On Log. Due to the accuracy of the MVDS, use the MVDS normal display screen as the transmitter primary metering system. Use the transmitter analog meters as a secondary metering system as required.

3-106. OVERLOADS. Four transmitter parameters are monitored for overloads by the transmitter controller and the MVDS: control grid bias current, screen current, PA VSWR, and plate current. If a single or a series of overloads occur: 1) the transmitter will cycle off-the-air, 2) the type of overload(s) will be displayed in the lower right-hand corner of the normal display screen with the most recent displayed at the bottom (refer to Figure 3-4), and an OVERLOAD LOG will be printed by the MVDS. If the overload clears, the transmitter will cycle on-the-air and the overload display will remain until the OVERLOAD reset switch is depressed.

3-107. TOLERANCE HIGHLIGHTING. If one of the transmitter parameters exceeds the limits of the customer configuration screen (example: low plate voltage), the value of the out-of-limit parameter will be highlighted (displayed in reverse video) on the normal display screen (refer to Figure 3-5). The CONDITION line will display the status of the transmitter (example: PA POWER LOW) and the DIAGNOSIS line will display the reason for the condition (example: LOW PLATE VOLTAGE).

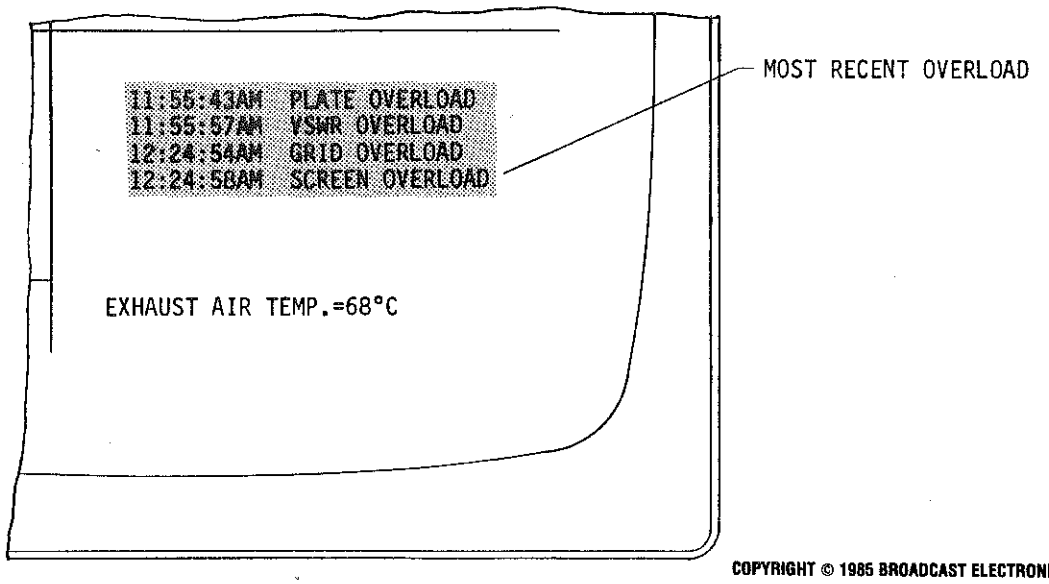

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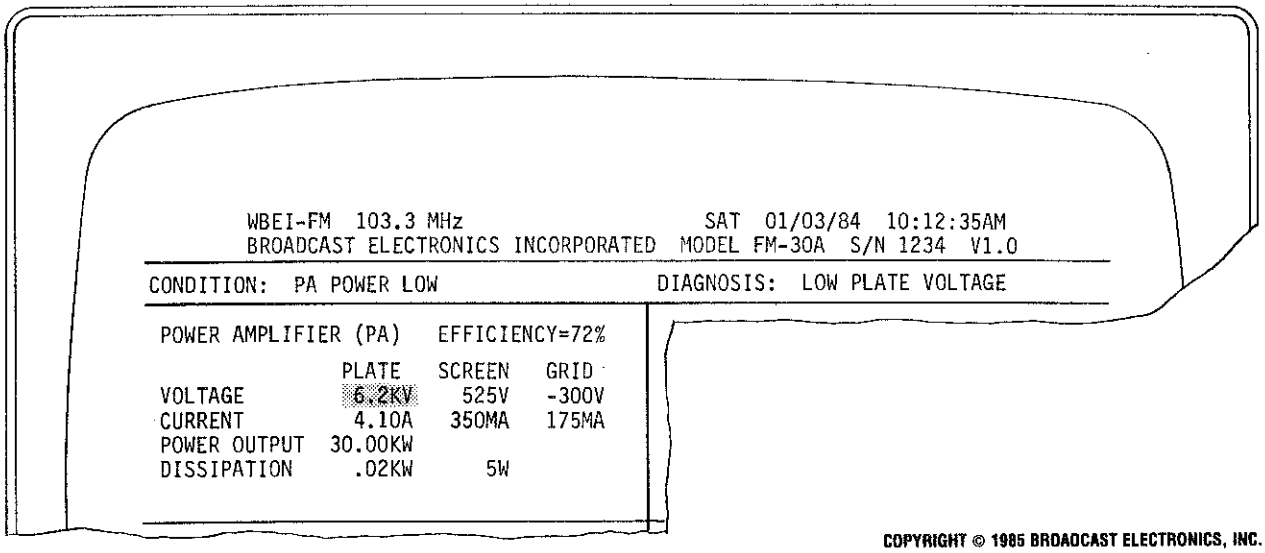
FIGURE 3-4. OVERLOAD DISPLAY



597-0036-13

FIGURE 3-5. TOLERANCE HIGHLIGHTING

3-108. NON-VOLATILE MEMORY MONITORING. Software within the MVDS is designed to monitor the status of the non-volatile memory. In the event of non-volatile memory failure, the following message will appear in reverse video on the normal display screen above the CONDITION/DIAGNOSIS line.

"*** REPLACE NONVOLATILE MEMORY, X8 ***"

3-109. OPERATION OF THE BAR GRAPH SCREEN (Screen 2).

3-110. The second operating display screen is the bar-graph screen (screen 2). The bar-graph screen displays the transmitter parameters in bar-graph form which changes with the status of the transmitter. The display is especially valuable in tuning the transmitter for overall maximum efficiency and checking the basic transmitter operating parameters quickly.

3-111. PROCEDURE. To access and observe the operation of the bar-graph screen, proceed as follows:

3-112. With the monitor displaying the normal display screen, depress key 2↓. The bar-graph screen will appear on the monitor.

3-113. Refer to the following illustrations for a description of the bar-graph display.

FIGURE 3-6	FIGURE 3-7	
FM-30A	FM-1.5A	FM-5A
FM-35A	FM-3.5A	FM-10A

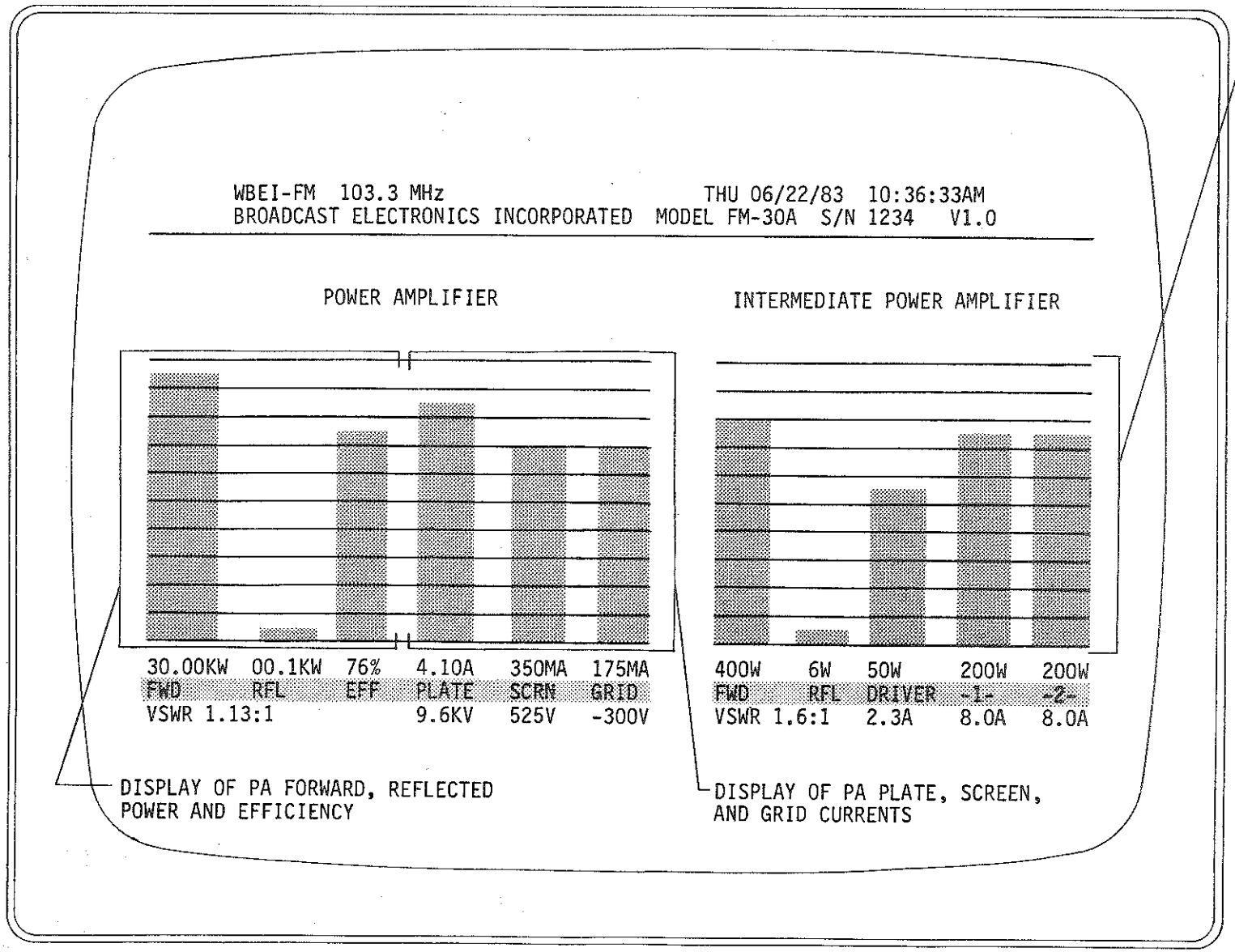
3-114. With the transmitter in operation, the bar-graphs will display a normal pattern of the transmitter parameters. If one of the displayed parameters exceeds the limits of the customer configuration screen (example: grid current), the parameter will be highlighted (refer to Figure 3-8).

3-115. MPU/DIGITAL CONTROLLER CONTROL.

3-116. With the MVDS option, the transmitter is equipped with two redundant and independent controllers: the transmitter digital controller and the MPU (microprocessor unit) controller which is incorporated into the MVDS. Both monitor transmitter parameters and completely control transmitter operations.

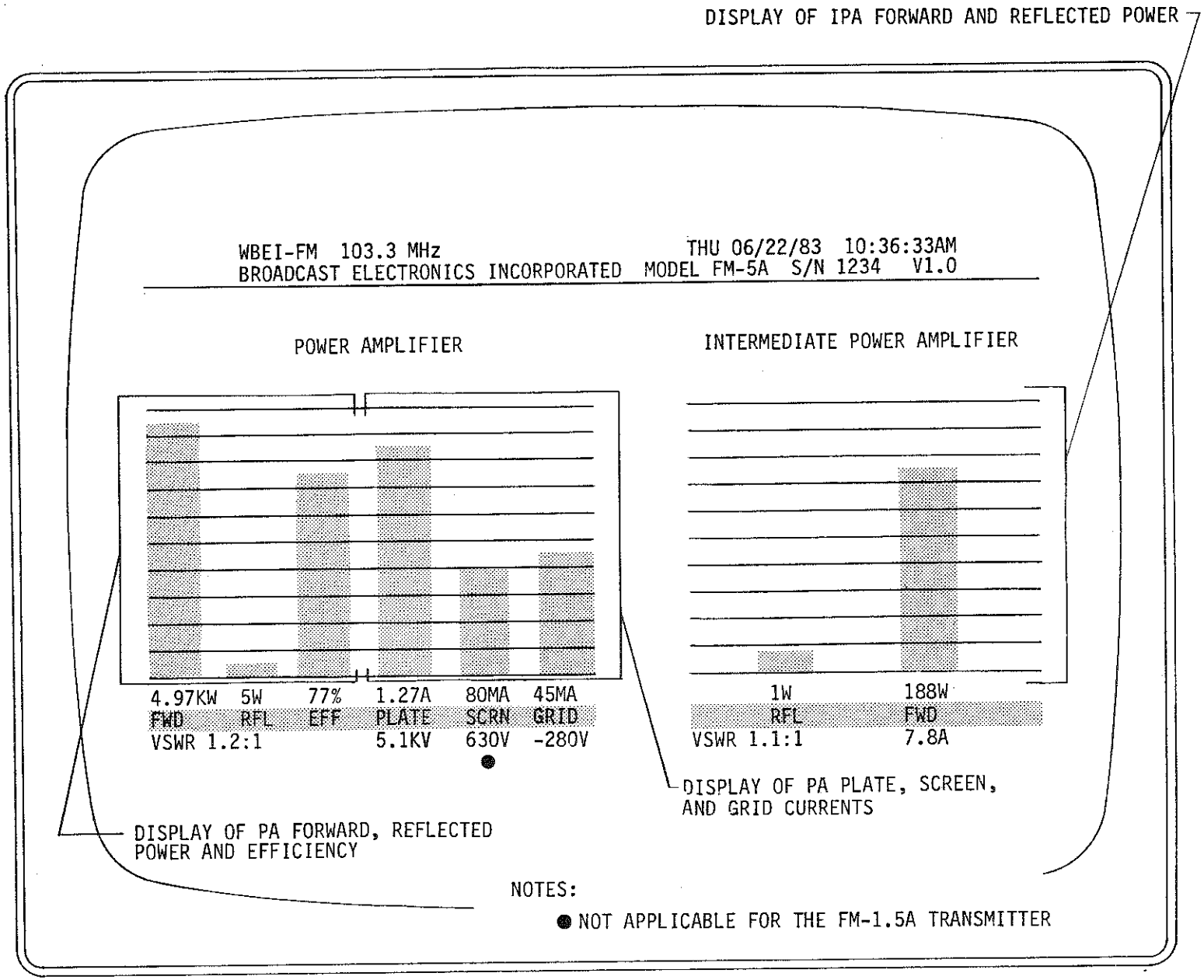
3-117. To operate the transmitter with the digital controller, operate switch S2 on the controller circuit board to CONT. With the digital controller, the filament warm-up time, tube cool-down time, overload recycle time, and the overload count limit are determined by the digital circuitry on the controller circuit board. The digital controller will control the transmitter operation with the MVDS displaying and diagnosing the transmitter parameters.

3-118. To operate the transmitter with MPU control, operate switch S2 on the controller circuit board to MICRO (MPU CONTROL will appear in the lower right-hand corner of the screen). With MPU CONTROL, the filament warm-up time, tube cool-down time, overload recycle time, and the overload count limit are determined by the values entered in the customer configuration screen. The microprocessor unit of the MVDS system will monitor and control transmitter operation and also display and diagnose the transmitter parameters. The controller circuit board will be by-passed until the microprocessor unit is disabled, then control will automatically be returned to the controller circuit board.



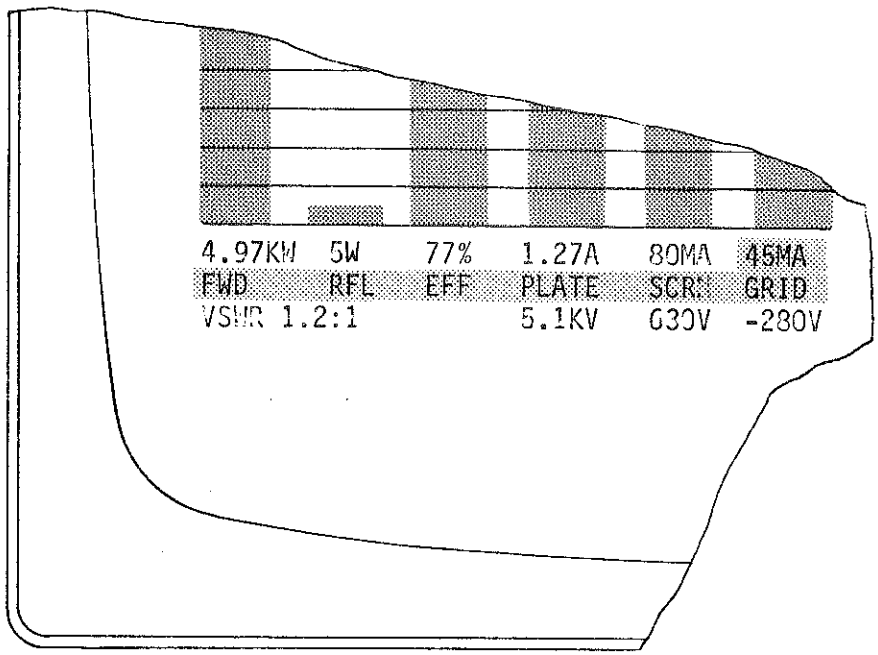
597-0036-14

FIGURE 3-6. FM-30A AND FM-35A BAR GRAPH DISPLAY SCREEN (Screen 3)



597-0036-15

FIGURE 3-7. FM-1.5A, FM-3.5A, FM-5A, AND FM-10A BAR GRAPH DISPLAY SCREEN (Screen 2)



597-0036-16

FIGURE 3-8. BAR GRAPH SCREEN HIGHLIGHTING

3-119. TRANSMITTER LOGS.

3-120. When a transmitter log is required, a copy of the normal display screen will be printed by the logging device. Logs may be requested by the operator at any time during the normal or bar-graph display screens (depress the L key) or provided automatically by the MVDS. The following list describes the conditions for an automatic log to occur:

1. A transmitter overload.
2. Operating the transmitter to ON.
3. Operating the transmitter to OFF.
4. An overload condition which deenergizes the transmitter to OFF.
5. An interval log which is determined by the customer configuration screen.

3-121. TRANSMITTER OPERATION WITHOUT MVDS.

3-122. Due to the dual controller design, the transmitter may be operated without MVDS if required. To operate the transmitter without MVDS, operate the MVDS ON/OFF switch to OFF. Control of the transmitter will automatically be returned to the digital controller.

NOTE WHEN MVDS IS DISABLED, ALL LOCAL AND REMOTE METER INDICATIONS WILL BE INACCURATE. TO CORRECT THE METER

NOTE INDICATIONS, REMOVE CABLE W7 FROM THE ANALOG-TO-DIGITAL CONVERTER CIRCUIT BOARD.

SECTION IV
THEORY OF OPERATION

4-1. INTRODUCTION.

4-2. This section provides the principles of operation for the Broadcast Electronics MVDS. An overall system description is presented first, followed by a detailed description of each circuit board.

4-3. GENERAL DESCRIPTION.

4-4. Refer to Figure 4-1 as required for the following discussion.

4-5. SYSTEM COMPONENTS.

4-6. The Broadcast Electronics MVDS is a video diagnostic system which is constructed of solid-state circuitry for maximum reliability. The system consists of the following items:

A. Circuit Boards:

1. 64K Memory Circuit Board
2. Analog/Digital Circuit Board
3. Input/Output Circuit Board
4. Central Processing Unit (CPU) Circuit Board
5. Video Display Module (VDM) Circuit Board
6. EMI Filter Circuit Board
* 7. Controller Circuit Board
8. Motherboard

* Supplied with the standard transmitter controller

B. System Keyboard

C. Video Monitor

D. Power Supply

4-7. 64K MEMORY CIRCUIT BOARD. The 64K memory circuit board provides all the read only memory (ROM) and the random access memory (RAM) for the MVDS system. The ROM is implemented through EPROMS (erasable programmable read only memory) which provide a permanent memory storage location for the system software. The RAM provides the microprocessor with temporary memory storage.

4-8. ANALOG/DIGITAL CIRCUIT BOARD. The Analog/digital circuit board converts analog transmitter samples to digital codes through CMOS analog-to-digital integrated circuits. The digital codes are stored within the analog-to-digital converter built-in memory and accessed by the microprocessor when required.

4-9. INPUT/OUTPUT CIRCUIT BOARD. The input/output circuit board provides data and control communication between the microprocessor and the keyboard, the controller circuit board, and the logging devices. Parallel input and output ports are provided for the controller circuit board. A parallel and serial port are provided for logging devices with one serial port dedicated to the system keyboard.

4-10. CPU CIRCUIT BOARD. The CPU circuit board is the main control element for the MVDS. The CPU contains a Z-80 microprocessor which executes the system software. The CPU accesses and routes data into and out of the system circuit boards.

4-11. VDM CIRCUIT BOARD. The VDM is a Z-80 based microprocessor circuit board that accepts data and commands from the CPU. In response to CPU commands and data, the VDM generates the composite video and synchronization pulses required by the video monitor.

4-12. EMI FILTER CIRCUIT BOARD. The EMI filter circuit board processes all keyboard and peripherial device inputs and outputs to minimize susceptibility to electromagnetic interference.

4-13. CONTROLLER CIRCUIT BOARD (Supplied with the standard Transmitter Controller). When the microprocessor is in control of the transmitter (MPU CONTROL), the controller circuit board provides the MVDS with transmitter indicator and switch status information. Also, control lines are routed through the controller circuit board which allows the microprocessor to operate the switch indicators, LED display, and control relays when required.

4-14. MOTHERBOARD. A communication network between the MVDS circuit boards is implemented through the motherboard. The motherboard interconnects the CPU, the 64K memory circuit board, the VDM circuit board, the analog/digital circuit board, and the input/output circuit board.

4-15. SYSTEM KEYBOARD AND VIDEO MONITOR. The keyboard and the video monitor provide communication between the operator and the MVDS. The operator communicates to the MVDS through keyboard commands which are processed by the microprocessor. The MVDS communicates to the operator through transmitter parameter displays on the video monitor.

4-16. POWER SUPPLY. The power supply provides all MVDS operating voltages and is completely independent of the standard transmitter controller power supply for greater reliability.

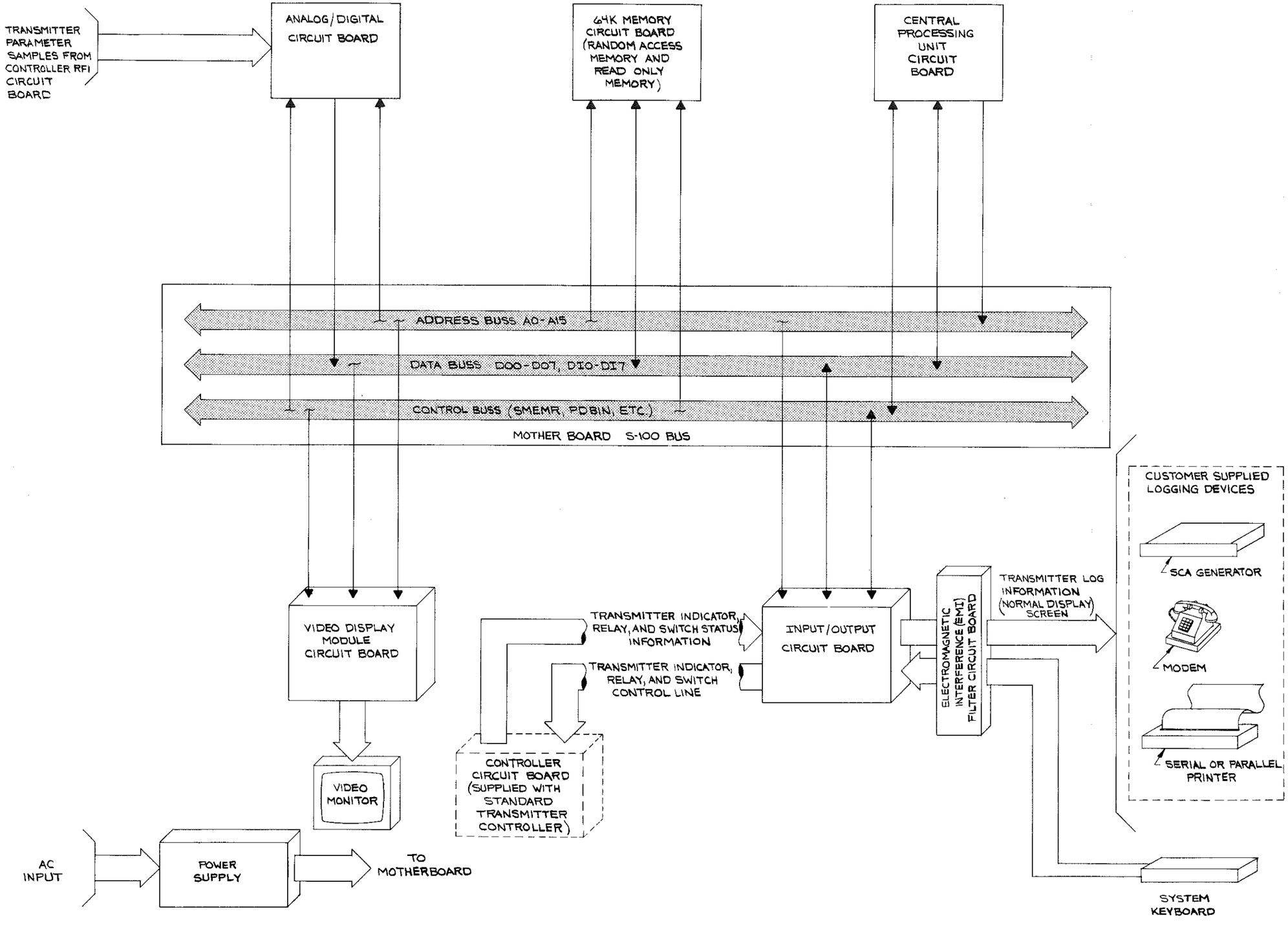


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FIGURE 4-1. MVDS BLOCK DIAGRAM

4-17. SYSTEM COMMUNICATION.

4-18. The MVDS operates under the direction of a Z-80 based microprocessor which is located on the CPU circuit board. The microprocessor responds to a set of instructions from a computer program which is stored in ROM on the 64K circuit board. Each instruction in the program has a specific location and a unique address within the memory. The microprocessor operates by: 1) accessing an instruction from the computer program, 2) processing the instruction, 3) routing data to or from the appropriate device.

4-19. Communication for microprocessor operation is provided by an S-100 bus which is implemented on the motherboard. The S-100 bus contains three communication buses: the address bus, the data bus, and the control bus.

4-20. The address bus transmits a 16-bit binary code from the CPU which identifies a specific device and memory location. The CPU can address memory on the 64K circuit board, analog/digital circuit board, VDM circuit board, or the input/output circuit board.

4-21. The data bus, which works with the address bus, carries information or data. The data bus is divided into two parts, Data In and Data Out. Data In is information entering the CPU from a location identified by the address. Data Out is information from the CPU to a location identified by the address.

4-22. The control bus carries control signals between the CPU and the MVDS circuit boards. Examples of these signals are the Read strobe and the Write strobe. The Read strobe indicates the CPU is in a mode to accept data that is present on the Data In bus. The Write strobe indicates the CPU is in a mode to transmit data on the Data Out bus. Both signals require a simultaneous address with active information on a data bus.

4-23. The microprocessor communicates with the controller circuit board, keyboard, and the logging devices via the input/output circuit board. Keyboard and controller circuit board information are accessed from the input/output circuit board by the microprocessor when required. Log and transmitter control information from the microprocessor is applied to the peripherial devices and controller circuit board through ports on the input/output circuit board.

4-24. DETAILED DESCRIPTION.

4-25. 64K MEMORY CIRCUIT BOARD.

4-26. GENERAL. The 64K memory circuit board provides both read only memory (ROM) and random access memory (RAM) for the MVDS system (refer to Figure 4-2). ROM, as the name implies, can only be read by the microprocessor. RAM is a type of memory that can be written into, changed, and read by the microprocessor.

4-27. The ROM is implemented through EPROMs which store 2048 bytes (eight bits equals one byte) of information. The EPROMs provide a permanent memory storage location for the MVDS control program. The control program directs the actions of the microprocessor and is electrically programmed into the EPROMs. Once programmed, the EPROM can only be erased by ultra-violet light. A sticker is placed over the window of the EPROM to prevent accidental erasing.

4-28. The RAM functions as temporary memory storage for the microprocessor. Two types of RAM are located on the 64K memory circuit board: volatile and non-volatile.

4-29. The volatile RAM is implemented through RAM integrated circuit X1 which stores 2048 bytes of information and provides the microprocessor with temporary data storage. This type of RAM is not battery supported and the stored data will not be retained when power is deenergized.

4-30. The non-volatile RAM is implemented through E^2PROM X8 which stores 2048 bytes of information and provides a memory location for the customer configuration screen data. This special type of RAM is not externally battery supported, however the stored information will be retained when power is deenergized. Therefore, the customer configuration screen data will not need to be re-entered after a power failure.

NOTE DI (DATA IN) REFERS TO DATA INPUT TO THE MICROPROCESSOR AND DO (DATA OUT) REFERS TO DATA OUTPUT BY THE MICROPROCESSOR.

NOTE

4-31. OPERATION. All inputs and outputs (data in bus, data out bus, and address bus) from the 64K memory circuit board are buffered by non-inverting tri-state bus drivers (refer to schematic 908-0017). The tri-state drivers are active only when the control signal is a logical LOW state. U14 buffers address lines AØ through A7 and U15 buffers A8 through A15. U16 buffers data out lines DOØ through DO7 and U17 buffers data input lines DIØ through DI7.

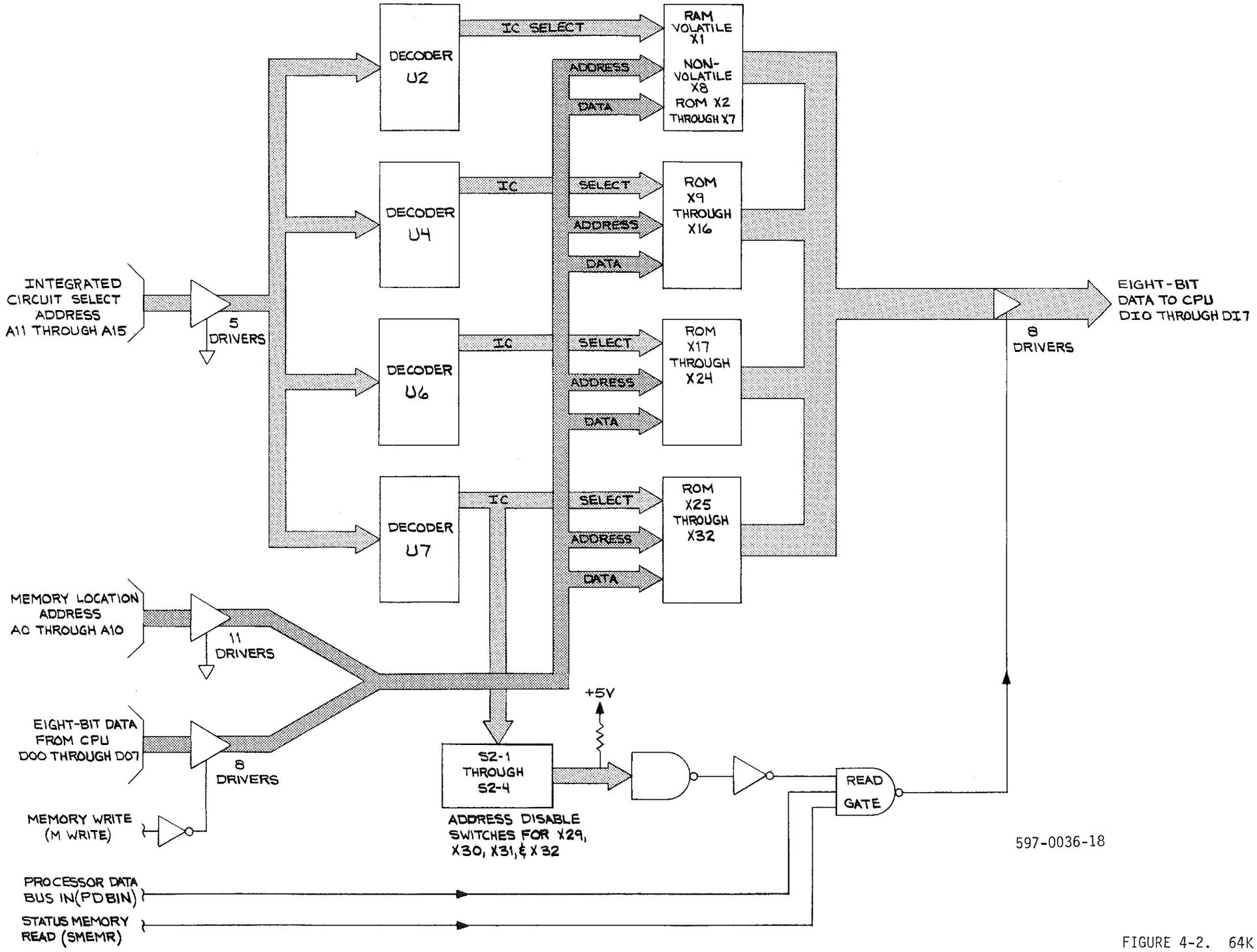

FIGURE 4-2. 64K MEMORY CIRCUIT BOARD BLOCK DIAGRAM

4-32. When the microprocessor requests or writes data from the memory circuit board, the particular memory location is selected with address lines AØ through A10 and the particular RAM or ROM integrated circuit is selected with address lines A11 through A15. Address lines A11 through A15 are routed to address decoders U2, U4, U6, and U7. The decoders output a LOW which enables the proper memory device. Memory location address lines AØ through A10 are routed directly from the buffers to each memory device for internal decoding by each RAM or ROM integrated circuit.

4-33. Address Disable Switches. Switches S2-1 through S2-4 are used to disable the data in bus (data routed to the microprocessor) when an address for memory locations on EPROMs X29, X30, X31, and X32 is assigned to a memory device which is located on another MVDS circuit board. When one of the switches is closed and one of the EPROMs (X29, X30, X31, X32) is selected by U7, a LOW is applied to one of the inputs of U20A. U20A outputs a HIGH through inverter U21D to NAND gate U20B. U20B outputs a HIGH which disables the data in bus driver.

4-34. Writing Data Into Memory. When the microprocessor is required to write data into RAM integrated circuits X1 or X8, the integrated circuit address will be decoded by U2 and the memory location address will be applied through address lines AØ through A10. The MWRITE signal from the microprocessor will go HIGH, indicating the microprocessor is ready to write data into a memory location. U21 inverts the MWRITE signal and applies a LOW to data output driver U16 which allows data to be written into memory.

4-35. Reading Data From Memory. When the microprocessor requests data from RAM or ROM, the memory location and integrated circuit address will be decoded by a combination of internal and external logic. U20B functions as a read gate and NANDS the processor data bus in signal (PDBIN), the status memory read signal (SMEMR), and the output of U20A (address disable switches). The SMEMR and the PDBIN signals the processor is ready to read data from memory and the timing is correct to route data onto the motherboard data in bus. When the inputs to U20B go HIGH, a LOW is output to the data in bus driver (U17), allowing the microprocessor to read data from memory.

4-36. ANALOG/DIGITAL CIRCUIT BOARD.

4-37. GENERAL. The analog/digital circuit board provides digital transmitter parameter values for the video display (refer to Figure 4-3). Analog transmitter parameters are converted to eight-bit codes through CMOS analog-to-digital integrated circuits. The digital codes are stored in the analog-to-digital converter RAM memory. Access to the memory is provided by the address bus. If the memory is not addressed every 10.2 seconds, an automatic reset signal will be applied to the microprocessor.

4-38. OPERATION. Transmitter parameter samples from the controller RFI filter circuit board are applied through an RC filter and protection diodes. The filtered sample is applied through an amplifier stage to the input of the analog-to-digital converter.

4-39. Analog-To-Digital Converter and Support Circuitry. The analog-to-digital converter is a data acquisition system which consists of an analog-to-digital converter, an 8 channel multiplexer, an 8 X 8 RAM (storage for 8 eight-bit words), tri-state data drivers, address latches, and control logic. The converter accepts eight analog inputs and sequentially converts each input into an eight-bit binary code. The eight binary codes are then stored in the 8 X 8 RAM. The tri-state data drivers, control logic, and the address latches control the flow of data to the data bus.

4-40. Timing is provided by a 1 MHz clock pulse from U24A. Calibration of the analog-to-digital converter is provided by dc offset voltage. Precision -10V reference U16 establishes a voltage to offset voltage amplifiers U14A and U14B. The non-inverted -10V dc output of U14A and the inverted +10V dc output of U14B are applied to all analog-to-digital converters through potentiometers and jumpers. This calibration is performed at the factory and is not considered a field adjustment.

4-41. Addressing The Memory. When the microprocessor requests data from the analog-to-digital memory, the memory location address is applied through address lines AØ through A2 and buffer U21 to each of the analog-to-digital converters. The three lines have eight combinations of logical states which the converter decodes and selects one of the eight memory locations.

4-42. Address line A5 will go LOW and be inverted by NAND gate U18A. Address line A8 will also go LOW and be inverted by U17A and NANDed at U18B with a HIGH from A7. Address lines A9 through A15 will go HIGH and be NANDed at U20 with a HIGH from U17B. U20 will output a LOW which is inverted HIGH by U17C. The HIGH from U17C is NANDed at U19A with a HIGH from the status memory read (SMEMR) signal, a HIGH from line A6, and a HIGH from U18A.

4-43. The analog-to-digital converter will be selected by address lines A3 and A4. Address lines A3 and A4 and a LOW from U19A are routed to converter address decoder U23. U23 decodes the BCD (binary coded decimal) address and outputs a LOW to enable the proper analog-to-digital converter.

4-44. Automatic Microprocessor Reset. As long as the microprocessor routes an active address to decoder U23, the decoder will periodically apply a LOW to automatic reset timer U25. This pulse prevents the reset timer from biasing transistor Q1 on. If the decoder does not receive an active address, a continuous HIGH will be applied to the reset timer. After 10.2 seconds, the timer will output a HIGH which biases Q1 on. This pulls the reset line LOW and resets the microprocessor.

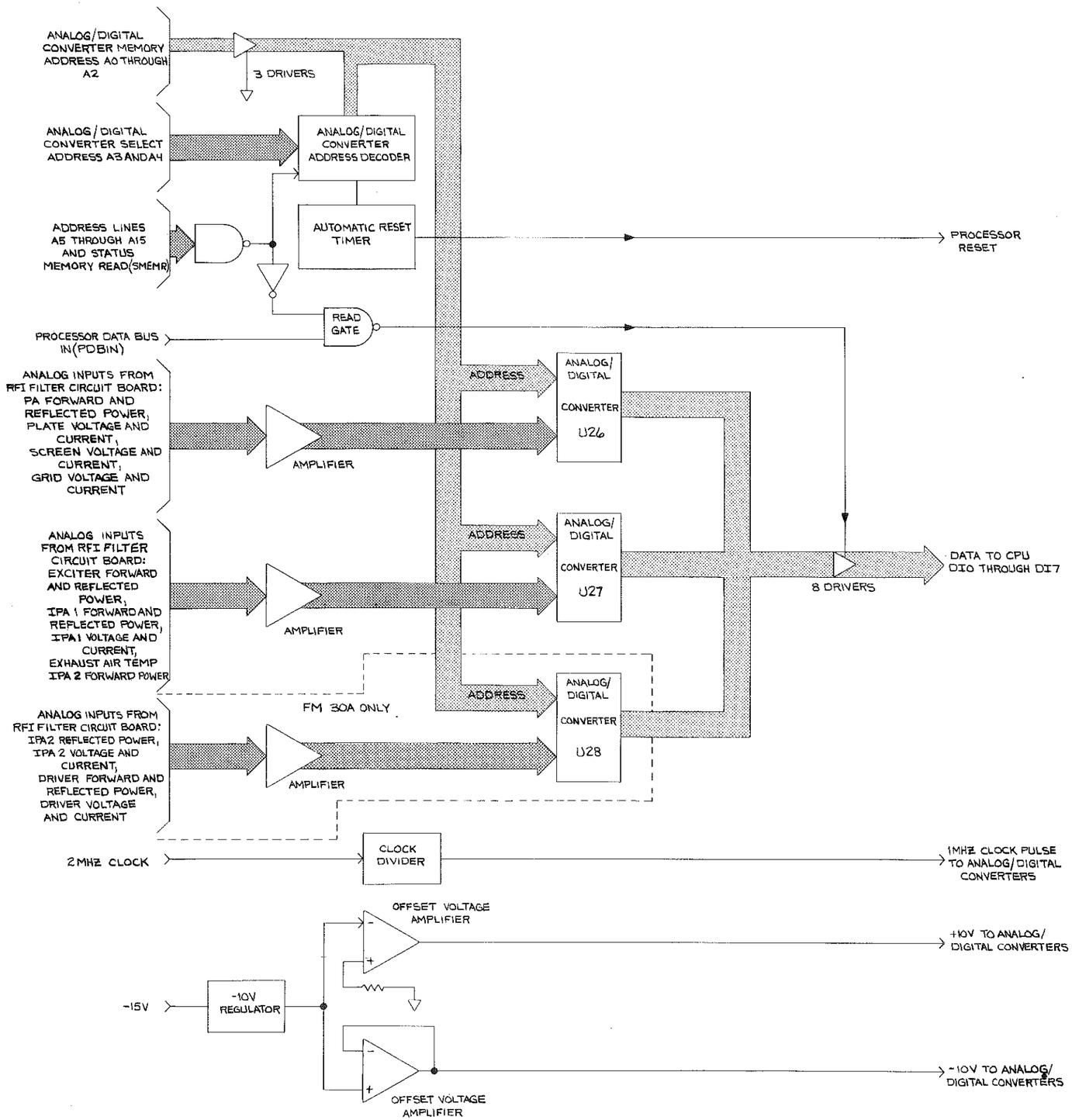

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FIGURE 4-3. ANALOG/DIGITAL CIRCUIT BOARD BLOCK DIAGRAM

4-45. Reading The Data. During the addressing sequence, the processor data bus in (PDBIN) signal will go HIGH, indicating timing is correct for data transfer. The HIGH from PDBIN is NANDed with a HIGH from the inverted output of U19A at read gate U18C. U18C will output a LOW to line driver U22, allowing the microprocessor to read data from the addressed memory location.

4-46. INPUT/OUTPUT CIRCUIT BOARD.

4-47. GENERAL. The input/output circuit board provides data and control communication between the microprocessor and the keyboard, the controller circuit board, and the logging devices. The input/output circuit board houses seven communication ports, address decoding logic, read and write circuitry, a controller circuit board monitor circuit, the 24-Hour clock, and the MPU (microprocessor unit) control request circuit.

4-48. OPERATION. Communication ports U11, U12, and U13 (refer to Figure 4-4) communicate with the keyboard and serial logging devices. The serial ports are referred to as universal asynchronous receiver/transmitters (UART). The UARTs contain four types of internal circuits: data exchange, control, status, and operation support.

4-49. The data exchange circuitry receives and transmits data between the microprocessor and the external devices. The control circuitry communicates microprocessor commands to the UART while the status circuitry communicates UART and external device logic conditions back to the microprocessor. The operation support circuitry provides internal clock information which allows the UART to operate at a rate that interfaces with the device with which it communicates.

4-50. The microprocessor addresses the UART in two different ways. The microprocessor can check the status of the UART for data present (example: keyboard information that is entered into U11) or enable the UART to route data to the peripherial device.

4-51. Parallel ports U7, U8, and U9 communicate transmitter indicator status and control information which is routed through the controller circuit board. Parallel port U1 (Centronics) communicates with a home computer type parallel printer.

4-52. The parallel ports contain internal information registers and control circuitry. Information routed to a parallel port is stored in four internal registers. The control circuitry directs the flow of the information to and from the registers. Information is accessed by the microprocessor by addressing the correct port and information register.

4-53. Addressing. Address decoding is performed by U10, U18, and U20. The address is applied through lines AØ through A7. An address is routed to the decoding logic through bidirectional bus lines DBØ through DB7 when the processor synchronization (PSYNC) line is pulsed HIGH. The PSYNC is inverted LOW by U31A which enables address buffer U32. U23A inverts the PSYNC line again and provides a clock pulse for the address latches.

4-54. The microprocessor can address several devices on the input/output circuit board. The following list describes the address lines for each device.

DEVICE	ADDRESS DESCRIPTION
Serial Port	Line AØ selects the data/status. Lines A2 and A3 select the particular serial port.
Parallel Port	Lines AØ and A1 select the information register. Lines A2 through A4 select the particular parallel port.
24-Hour System Clock	A logical combination of lines AØ through A5.
MPU Control Request Circuit	A logical combination of lines AØ through A6.

4-55. When the microprocessor routes an address to the decoding logic, the states of lines DBØ through DB3 will be latched into U10. Address lines A8 through A15 will go HIGH and be NANDed at U33. The output of U33 will go LOW and be inverted by U27A. Line DB4 and a HIGH from inverter U27A are routed to U18. Lines DB5 through DB7 are partially decoded at U28A and U30B, and routed to latch U18.

4-56. Latch U10 will output: 1) the proper register enable for the parallel ports or the status/data mode for the serial devices, 2) one-half of the communication port address to U20. U18 outputs the other one-half of the communication port address to decoder U20. U20 decodes the BCD (binary coded decimal) address and applies a LOW to enable the proper communication device.

4-57. Write Logic. When the microprocessor is required to write data to one of the communication ports, the microprocessor synchronization (PSYNC) line will pulse HIGH, allowing the address of the communication port to be decoded. The PSYNC will return to a LOW state and be applied through a series of inverters as a HIGH to U30A.

4-58. U30A NANDs the PSYNC signal, the status memory read signal (SMEMR), and the Q2 output of U18. The SMEMR will be LOW and inverted HIGH by U31B. The Q2 output of U18 will go HIGH, allowing U30A to output a LOW to inverter U31F and data-out bus driver U34. The memory write (MWRITE) line will go HIGH and be NANDed at U19A with a HIGH from inverter U31F. U19A will output a LOW to enable the write function of the correct communication device.

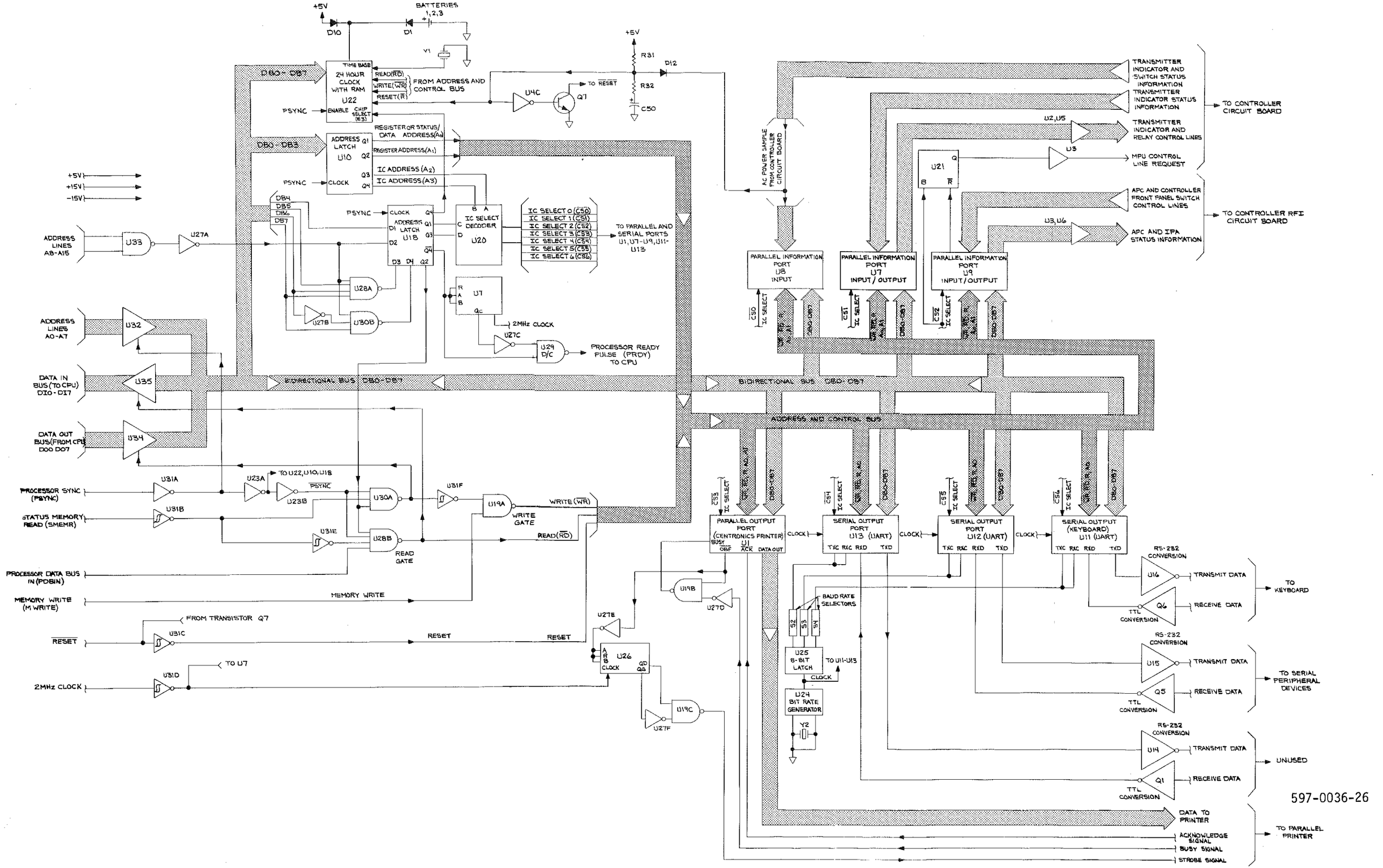

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FIGURE 4-4. INPUT/OUTPUT CIRCUIT BOARD SIMPLIFIED SCHEMATIC

4-59. Read Logic. U28B functions as a read gate and NANDs the processor synchronization (PSYNC) pulse, the status memory read signal (SMEMR), the processor data bus in (PDBIN) signal, and the Q2 output of U18. When the microprocessor is required to read data from a communication port, the PSYNC line will pulse HIGH, allowing the address to be decoded. The PSYNC will return to a LOW state and be applied through a series of inverters as a HIGH to U28B. The SMEMR signal, the PDBIN signal, and the Q2 output of U18 will go HIGH indicating the microprocessor is ready to route data onto the data-in bus. U28B will output a LOW which enables the read function of the communication port and data-in bus driver U35.

4-60. UART Output Interface Circuitry. In order for the UART to transmit or receive data from an external device, the data must be converted to the correct voltage levels. Amplifiers U14, U15, and U16 convert the transmit data to RS-232 levels. Transistors Q1, Q5, and Q6 convert the RS-232 receive data from the external devices back to TTL levels for UART operation.

4-61. Parallel Printer Port (Centronics) Control Logic. The Centronics control logic on the input/output circuit board provides a start pulse and a wait state for the printer. When Centronics port U1 is required to route data to the printer, U1 will output a LOW at $\overline{OBF}$ (output buffer full) to shift register U26. U26 will output a signal to NAND gate U19C which outputs a start pulse to the printer.

4-62. While printing data, the printer will output a busy signal to inverter U27D. U27D outputs a LOW which is NANDed with a LOW from the $\overline{OBF}$ at U19B. U19B routes a HIGH to the busy input of Centronics port U1 which operates the port into a wait state.

4-63. Controller Circuit Board Monitor Circuit. An ac power sample from the controller circuit board is applied to parallel information port U8. If power to the controller circuit board is disabled, a ground is applied to D12 which pulls R31 and the reset line to U22 LOW. The LOW is inverted by U4C and biases on transistor Q7. Q7 pulls the reset line LOW which resets the microprocessor and all the communication ports. When power is returned, the +5V charges through R31 and C50 which applies a 0.5 second reset pulse to the microprocessor. The reset pulse allows the communication ports to stabilize data before the microprocessor resumes operation.

4-64. 24-Hour Clock. The 24-Hour clock is generated on integrated circuit U22. Integrated circuit U22 contains a complete clock and calendar system, address decoding logic, 14 bytes of clock/calendar RAM, and 50 bytes of general purpose RAM.

4-65. Crystal oscillator Y1 provides a time base for clock operation. Back-up power is provided by three seriesed batteries. U22 operates by continuously generating clock and calendar data. The data is converted to a parallel format and stored in the clock/calendar RAM.

4-66. The microprocessor addresses U22 through lines DBØ through DB6. The address is decoded through a combination of internal logic and external decoding logic U33, U30B, and latch U18. U18 supplies a HIGH which enables U22 and a LOW (at $\overline{Q4}$) to shift register U17 and NAND gate U29. U29 outputs the processor ready pulse (PRDY) to the microprocessor. The PRDY pulse instructs the microprocessor to wait before accessing the memory location.

4-67. The microprocessor accesses the clock and calendar data by applying the correct address to the decoding logic. Once the address is decoded, a LOW from read gate U28B will enable the read function of U22, allowing the data to be routed on the bidirectional bus. The microprocessor also writes overload and time data into the 50 bytes of general purpose RAM. The write function is enabled when the proper address is decoded and a LOW is applied from write gate U19A.

4-68. MPU Control Request Circuit. In order for the MVDS to control the transmitter (MPU Control), the microprocessor must receive control from the controller circuit board. The microprocessor gains control of the transmitter by continuously addressing and enabling (applying a LOW) parallel port U9 and the correct information register. Port U9 routes a HIGH to the active-LOW reset of U21. U21 outputs a HIGH to the logic on the controller circuit board. The logic transfers control to the microprocessor if the switch on the controller circuit board is operated to the MICRO position.

4-69. CENTRAL PROCESSING UNIT CIRCUIT BOARD (CPU).

4-70. The CPU circuit board is the central communications and decision making element in the MVDS. At the core of the CPU circuit board is the Z-80A microprocessor chip. All the remaining circuitry on the circuit board aids in routing data, supports operation of the microprocessor chip, and interfaces the circuitry to the S100 bus system (see Figure 4-5).

4-71. OPERATION. The Z-80A microprocessor has four output signals that indicate what the microprocessor is doing at any instant (refer to Schematic 919-0059). These four outputs are used to synchronize external logic to steer data as required by the microprocessor. These outputs are: 1) input or output request ($\overline{IORQ}$), 2) memory request ($\overline{MREQ}$), 3) write ($\overline{WR}$), and 4) read ($\overline{RD}$). These signals are gated together according to the following combinations to form the indication functions:

A. SOUT (status output) = $(\overline{WR})(I\overline{ORQ})$*. Indicates that the processor is outputting data to a port (S-100 bus pin No. 45). During this type of instruction execution, data is output on the data out bus, the port address is output on the address bus, and the processor write pulse ($\overline{PWR}$) provides timing to the external logic.

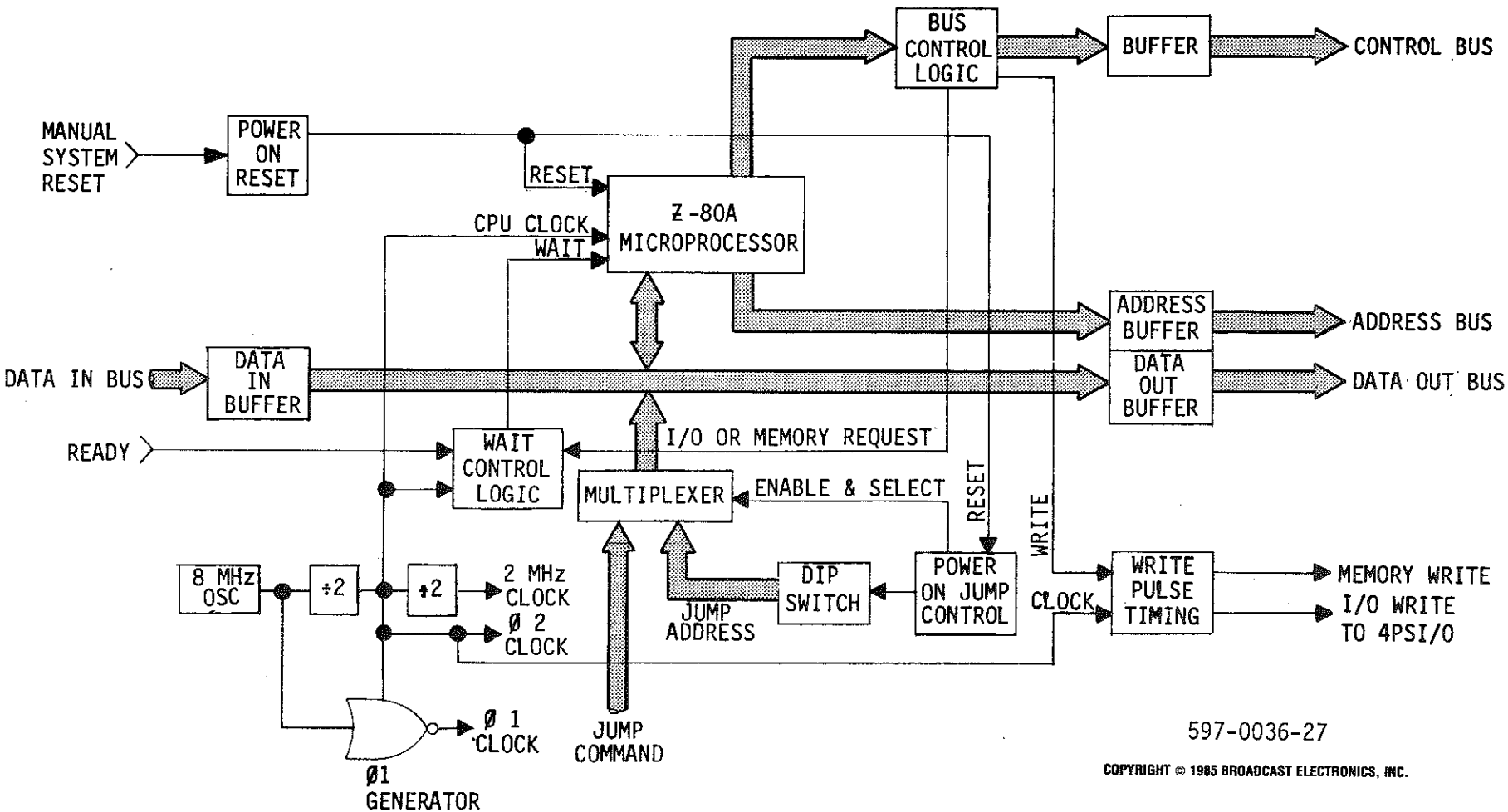


FIGURE 4-5. CPU CIRCUIT BOARD BLOCK DIAGRAM

B. SINP (status input) = $(\overline{RD})(\overline{IORQ})$. Indicates that the processor is accepting data from a port (S-100 bus pin No. 46). During this type of instruction execution, data is input on the data in bus while the address is output on the address bus. The processor data bus in signal (PDBIN) provides timing to the external logic.

C. SMEMR (status memory read) = $(\overline{RD})(\overline{MREQ})$. Indicates that the processor is reading data from memory (S-100 bus pin No. 47). During this operation, the address of the data desired is output from the microprocessor on the address bus, and the data is read in on the data input bus. The processor data bus in signal (PDBIN) provides timing to the external memory element.

There are many operations in which the microprocessor reads data from memory, and this operation is by far the most frequent. As all instructions for the microprocessor are stored in memory, each instruction must be read, one at a time, as each instruction is executed. The first operation of each instruction cycle is to read a specific instruction from memory. The microprocessor may also read data from memory during the execution of an instruction, depending on the instruction itself.

D. MWRITE (memory write) = $(\overline{PWR})(\overline{MREQ})$. Indicates that the microprocessor is writing data to memory (S-100 bus pin No. 68). During this operation, data is output on the data out bus, and the address in memory where the data is to be stored is output on the address bus.

* NOTE: The expression $(\overline{WR})(\overline{IORQ})$ indicates a logical ANDing of $\overline{WR}$ and $\overline{IORQ}$.

4-72. Power-On Jump. The power-on jump instruction causes an automatic jump to a switch-specified address upon power on or reset. The logic for this feature is composed of integrated circuits U13, U14, U21, and switch S1. Integrated circuit U13 is a quad, edge-triggered, type-D latch which is used as a three-bit shift register. U13 is clocked by the output of a quad NAND gate section of U6. When U13 is reset by the power-on reset logic, it causes a series of three bytes (8 bits X 3) of information to be placed on the CPU circuit board data bus in response to the first three read cycles that the CPU executes.

4-73. The first three read cycles after a reset to the microprocessor are the instruction fetch cycles for the first instruction to be executed. Integrated circuits U14 and U21 are multiplexer chips with inverting tri-state outputs. During each of the first three read cycles, these multiplexers put data onto the CPU circuit board data bus. This information consists of the inverse of either the A or B inputs to U14 and U21, depending on the position of switches S1A through S1H.

4-74. The reset pulse begins the power-on jump by resetting both the microprocessor chip and all states of U13. This causes all Q outputs to go LOW and all $\overline{Q}$ outputs to go HIGH. Because each successive read cycle will clock a HIGH into the next stage, three read pulses will cause all the stages to have a HIGH on their Q output and a LOW on the $\overline{Q}$ output.

4-75. The first microprocessor read cycle will read the complement of the A inputs to U14 and U21 into the microprocessor. This is a jump command. At the end of the first read cycle, the first stage of U12 will change states, changing the select input to each multiplexer.

4-76. The second microprocessor read cycle will read all LOW states into the microprocessor as all B inputs are HIGH. The position of switches S1A through S1H does not affect this second word because the $\overline{Q}$ output of the second stage is HIGH. At the end of the second read cycle, $\overline{Q}$ of the second stage is clocked LOW.

4-77. The third microprocessor read cycle will read the high-order byte (8 bits) of the jump command into the microprocessor. On bits where the switch input is open, a HIGH will be input to the multiplexer and a LOW will be placed on the CPU circuit board data bus. On bits where the switch input is closed, a LOW will be input to the multiplexer and a HIGH will be placed on the CPU circuit board data bus. At the end of the third read cycle, the last stage of U13 changes stages. This causes the automatic power-on jump (AUTOJ) cycle to be terminated. Program execution will now begin at the new address.

4-78. Write Pulse Timing. The processor write pulse ($\overline{PWR}$) provides timing to external logic for outputting data. The circuit operates as follows: Quad type-D latch U4 is connected as a three-bit shift register. When a write pulse from the microprocessor occurs, the pulse is shifted into the first section of U4 and causes the $\overline{Q}$ output to go LOW. Two clock pulses later, the Q output of the third stage of U4 will go high and terminate the $\overline{PWR}$ pulse. This forms a $\overline{PWR}$ pulse 0.5 microseconds long, occurring within the period of the microprocessor write pulse.

4-79. Wait Logic. U8, U1 and Y1 form a 4 MHz clock circuit which acts as a frequency reference for the microprocessor chip (U12). This circuitry also forms the basis of the wait logic which allows the microprocessor to operate at a rate faster than the rate at which the input/output logic and memory circuits operate.

4-80. For an internally generated wait, the $\overline{Q}$ output of the first stage of quad type-D edge-triggered latch U2 is connected to the D input. In this configuration, it divides the clock frequency by 2. This 2 MHz signal, along with the 4 MHz signal, are routed to the S-100 bus to synchronization for the other system circuit boards.

4-81. The second and third sections of U2 are connected as a two-bit shift register. With Q of the second section gated with $\overline{Q}$ of the third section, a pulse generator is formed. A LOW-going pulse, one clock period wide is generated each time the D input of the second section goes HIGH. The D input is the result of the function D = ($\overline{MREQ}$) ($\overline{IORQ}$). Each time the microprocessor executes a cycle that involves access to memory, an input port, or an output port, one clock period pulse is generated at the output of U3. This pulse is applied to inverter U5 to form a negative-going pulse ($\overline{WAIT}$) at the input of the microprocessor.

4-82. Through this mechanism, one wait state is automatically inserted into the microprocessor timing for each memory access and each input/output access. This wait state allows the microprocessor to operate at 4 MHz with memory access and input/output timing operating at 2 MHz. This increases the system performance without the additional cost of higher speed memory and input/output logic.

4-83. The external ready inputs can also place the microprocessor into a wait condition for as long as the input signal remains present. The two external ready inputs are external equipment ready (XRDY) and processor ready (PRDY). Both signals are gated together by U3 and synchronized with the CPU clock by the fourth stage of U2. The output from U5 is then gated with the automatic wait state pulse and applied through U5 to the microprocessor. A LOW on either of the circuit board inputs will place the microprocessor in the wait mode for the duration of the LOW input.

4-84. VIDEO MONITOR DISPLAY CIRCUIT BOARD.

4-85. GENERAL. The video display module (VDM) is a fully self-contained microprocessor-based display terminal board that accepts ASCII data and commands from the CPU circuit board (refer to Figure 4-6). The VDM stores the data and generates both composite video and separate TTL levels for horizontal sync, vertical sync, and video output. The VDM is interfaced through the S-100 bus to the main processor CPU. A port informs the CPU when the VDM is ready to receive data.

4-86. The VDM utilizes a Z-80A microprocessor to perform the logic functions such as data storage, line feed, carriage return, cursor addressing, and scrolling. It also utilizes a CRT 5027 CRT controller integrated circuit to provide the scanning necessary for character display and provides timing to generate vertical and horizontal synchronization pulses and blanking. The VDM supplies both composite signals to the CRT and separate TTL level synchronization and timing.

4-87. A 8K X 8 EPROM memory stores the microprocessor program and a second 8K X 8 EPROM functions as a character generator to control the individual dots that form the characters on the CRT display. Additional memory includes a 2K X 8 RAM which is accessed by the microprocessor as required during program execution.

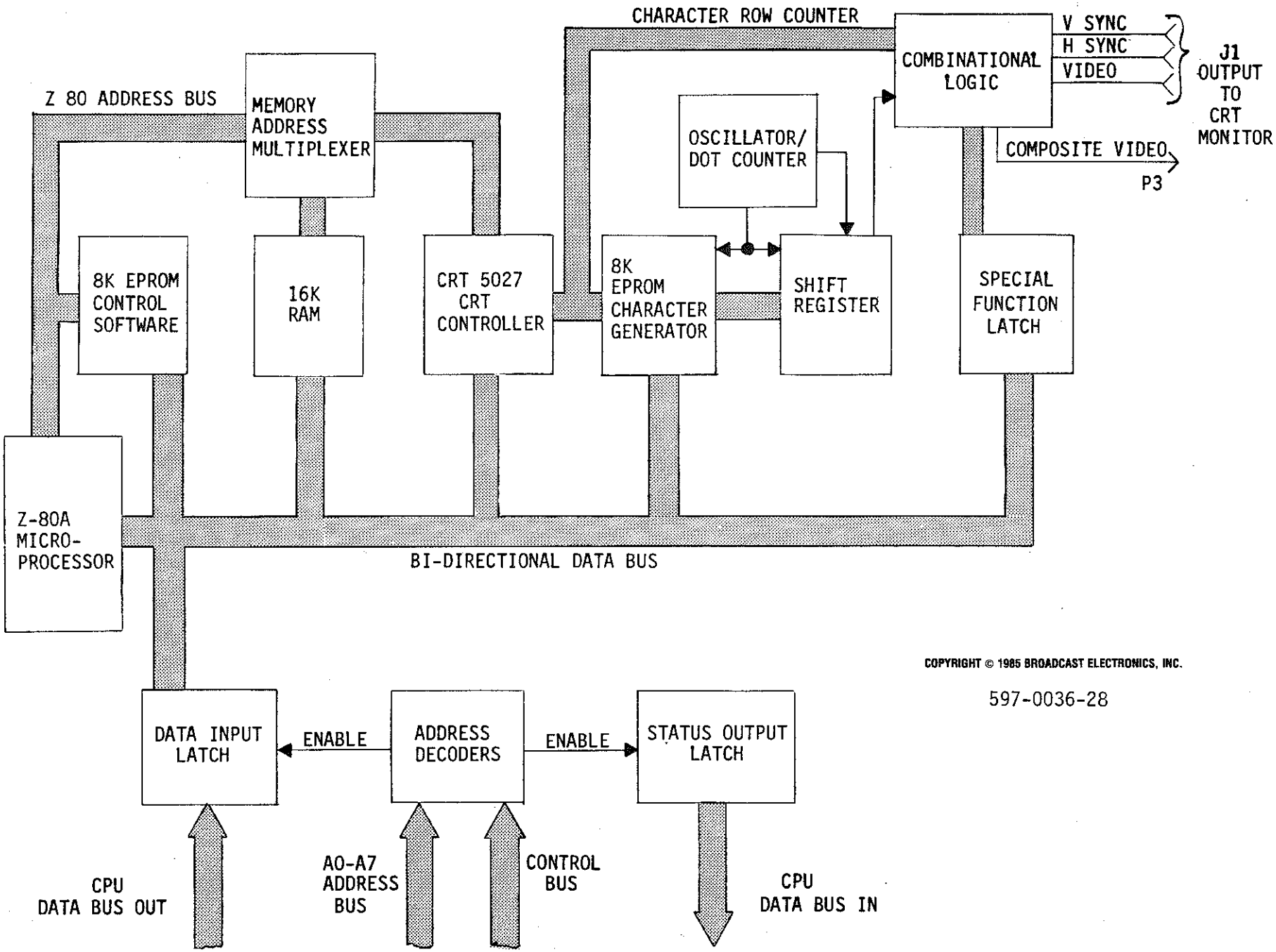


FIGURE 4-6. VDM CIRCUIT BOARD BLOCK DIAGRAM

4-88. OPERATION. Information from the microprocessor to the VDM is written to hexadecimal address port address F9 (refer to Schematic 919-0036). The port address is decoded by U21, U22, U31, and U32. The decoded port address is gated with the status out (SOUT) signal and the processor write ($\overline{PWR}$) signal from the CPU to U21 which generates strobes to U20 and U30. U21 also gates the status input (SINP) signal and the processor data-bus-in (PDBIN) signal inputs with the port number to enable tri-state line driver U19.

4-89. Data on the microprocessor data out bus is latched into U30 by the strobe from U21 and U20 generates an interrupt to the Z-80A (U11) in response to its strobe. In addition, U20 controls the status sent back to the microprocessor through U19 when hexadecimal port address F8 is read by the microprocessor. The port number is decoded by the same port decoding circuitry as the port address.

4-90. In response to the interrupt request generated by U20, the microprocessor chip (U11) inputs the data stored in latch U30 and analyzes the data. U11 can then store the data into the 16k RAM (U24, U25, U26, and U27) if required.

4-91. Integrated circuits U8, U10, U18, U34, and portions of U22 and U23 form a memory address multiplexer. Under control of U11, the microprocessor can address the RAM through the multiplexer, or CRT controller U9 can address the RAM.

4-92. Two gates of U14 and Y1 are connected as a crystal stabilized oscillator which generates a 14.43098 MHz reference frequency. This frequency is a "dot clock" which generates timing for CRT controller U9. In addition, U12 and U14 form a divide-by-nine counter which outputs a "character clock". These two clocks determine that each character position will be 9 dot positions wide.

4-93. The character clock output of U12 is routed to the dot counter carry input of U9. In addition, the dot counter carry signal is inverted and used to load data into U6, U13, and U29. U13 is a shift register that is loaded with parallel data from the character generator for each line of each character. It receives its first eight dots from character generator U28. The ninth dot will always be the same as the first because the H output and the serial input are connected together. The $\overline{H}$ output is pre-processed dot video as the shift register is clocked at the dot clock rate.

4-94. CRT controller chip U9 addresses RAM through the address multiplexer to scan across and down the screen as the sweep proceeds. Lines HØ through H6 address the horizontal characters, or the low order portion of RAM address. Output lines DRØ through DR4 address the vertical row, or the high order portion of RAM address.

4-95. The row address information is used as the low order portion of the address input for character generator U28. The high order portion of the address for the character generator is the lower seven bits of the word from RAM. The CRT controller chip address lines, the RAM, and the character clock latch the RAM data into U29. Therefore, the character generator U28 which then yields the dot pattern. This dot pattern is then loaded into shift register U13 and is shifted out as dot video.

4-96. CRT controller U9 also provides blanking, composite sync, vertical sync, and horizontal sync as outputs. The composite sync is gated in U36 and applied to latch U33 to generate a bus request-not ($\overline{\text{BUSRQ}}$) signal. Under normal conditions, the microprocessor (U11) will insert a HIGH in latch U33. This HIGH allows the microprocessor to access the data bus and the RAM only during sync pulse formation. In response to the $\overline{\text{BUSRQ}}$ input, U11 will output a bus acknowledge ($\overline{\text{BUSAK}}$) signal.

4-97. $\overline{\text{BUSAK}}$ signals the RAM address multiplexer that the microprocessor has suspended processing and has allowed CRT controller U9 to access the RAM address bus and the data bus to read information from RAM. When the composite sync pulse is output, the $\overline{\text{BUSRQ}}$ and therefore the $\overline{\text{BUSAK}}$ goes away, and the microprocessor is again allowed to access RAM.

4-98. Therefore, the microprocessor operates only during the low-going composite sync pulses, or when U11 writes a LOW into D7 of latch U33. With a LOW in U33, the latch output is gated with composite sync so that the microprocessor operation can not be suspended. The only time this occurs is when the microprocessor has a great deal of processing to perform. A clear screen function is an example of when a great deal of processing is required as all RAM must be cleared.

4-99. Integrated circuits U15 and U20 form a five-bit, divide-by-32 counter which operates from vertical sync. This counter generates an approximate 2 Hz signal which is used to generate a special effect when desired.

4-100. The highest order memory bit of the RAM data (D7) is used as an enhancement flag. This bit is loaded into U6 at the same time that U13 is loaded with dot information. The output of U6 indicates to the remaining logic circuitry which characters are to be enhanced. An example of enhanced characters are the reverse video characters that display the out-of-limit transmitter parameters. Active enhancement modes are controlled by the microprocessor which controls the output of latch U33. The following list details the meaning of each data bit.

DATA BIT	LATCH Q	EFFECT
4	7	Controls the gate to the $\overline{\text{BUSRQ}}$ input of the microprocessor.
4	2	Underlines the enhanced characters (unused).
3	5	Causes all video to be blanked.
2	6	Causes all enhanced characters to appear in reverse video.

4-101. The dot video is then inverted by U2, and depending upon the inputs to U3, the dot video may be inverted again. U3 is an exclusive OR gate which functions as a selective inverter. If pin 12 is LOW, the input will be output in a non-inverted condition. If pin 12 is HIGH, the input will in inverted.

4-102. The dot video from U3 is routed through another gate of U4 in which the video is gated with vertical sync which blanks the video during the vertical interval. The video is also gated with the blanking output of CRT controller U9 which blanks the video during the blanking portion of the horizontal sweep. The video is also gated with a third blanking signal through inverter U2 from U16. This signal gates together the enhancement flag from U6 and the blinking enhancement bit from U33. As the underline enhancement mode is not used in the MVDS, the fourth input to U16 is inactive.

4-103. Integrated circuit U17 gates together two different sets of conditions that can cause video reversal (used as a special effect to intensify or highlight a portion of the display screen). The first set of conditions generates the blinking underline cursor. U17 does this by gating together the blinking signal from U15, the cursor position from CRT controller U9, and the row 9 conditions. When all these conditions occur, the output of U17 will go HIGH, causing the video to be reversed in row 9 of the character designated by U9 as the cursor position.

4-104. The second set of conditions that generates reversed video involves the enhanced fields controlled by the microprocessor. When the enhancement flag is set and reverse video enhancement is selected, the output of U17 will go HIGH, causing the video reversal. Again, because underline enhancement is not used in the MVDS, the third input to U17 is not active.

4-105. The output circuit consists of transistor Q1 which mixes the composite sync from U9 with dot video from U4 to generate a 75 Ohm composite video output (video plus sync).

SECTION V

MVDS MAINTENANCE

5-1. INTRODUCTION.

5-2. This section provides maintenance information for the Broadcast Electronics MVDS.

5-3. SAFETY CONSIDERATIONS.

5-4. Low voltages are used throughout the MVDS circuit boards, however maintenance with power energized is always considered hazardous and caution should be observed. All high voltages used within the controller cabinet have been shielded, however do not touch any component within the controller cabinet with power energized. Good judgement, care, and common sense must be practiced to prevent accidents. The procedures contained in this section should be performed only by experienced and trained personnel.

5-5. If any MVDS maintenance requires removal of the controller cabinet or troubleshooting within the transmitter, refer to the applicable transmitter manual for safety and maintenance procedures. Never open the transmitter unless all primary power is disconnected.

5-6. MAINTENANCE.

CAUTION INADVERTENT CONTACT BETWEEN ADJACENT COMPONENTS OR CIRCUIT BOARDS WITH TEST EQUIPMENT CAN CAUSE SERIOUS DAMAGE TO THE MVDS.

CAUTION

5-7. PREVENTATIVE.

5-8. The preventative maintenance philosophy consists of regularly inspecting the MVDS for improperly seated circuit boards and semiconductors, and components damaged by overheating. Also, clean the circuit boards as required to prevent future failures.

5-9. ADJUSTMENTS.

WARNING NEVER OPEN THE TRANSMITTER UNLESS ALL PRIMARY POWER IS DISCONNECTED.

5-10. The following text provides procedures to adjust all controls associated with the MVDS. Adjustment procedures for each control are presented in the following order.

A. Input/Output circuit board adjustments.
B. Analog/Digital circuit board adjustments.

WARNING: DISCONNECT POWER PRIOR TO SERVICING

5-11. INPUT/OUTPUT CIRCUIT BOARD ADJUSTMENTS.

5-12. MVDS 24-HOUR CLOCK ADJUST (C2). The MVDS 24-hour clock control adjusts the clock frequency to provide accurate time. To adjust the control, refer to the following information.

5-13. Required Equipment. The following equipment is required to adjust the MVDS 24-hour clock control (C2).

A. Insulated adjustment tool, flat-tip (BE P/N 407-0083).

B. Frequency counter.

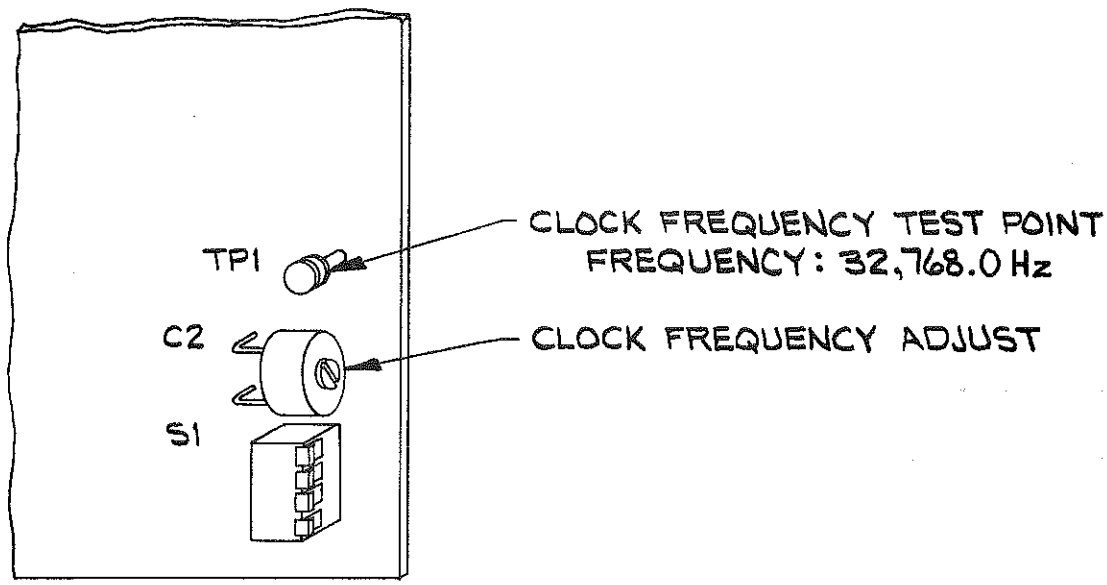
5-14. Procedure. To adjust the control, proceed as follows:

5-15. Apply power to the transmitter.

5-16. Refer to Figure 5-1 and connect a frequency counter to the clock frequency test point (TP1).

5-17. Adjust capacitor C2 until the frequency counter indicates 32,768.0 Hz.

5-18. Remove the frequency counter.



597-0036-19

FIGURE 5-1. INPUT/OUTPUT CIRCUIT BOARD CONTROL

WARNING: DISCONNECT POWER PRIOR TO SERVICING

5-19. ANALOG/DIGITAL CIRCUIT BOARD ADJUSTMENTS.

5-20. PA FORWARD POWER, PLATE VOLTAGE, AND PLATE CURRENT DIGITAL DISPLAY CALIBRATE (R43, R67, R94). To calibrate the values of PA FORWARD POWER, PLATE VOLTAGE, and PLATE CURRENT displayed on the normal display screen to the transmitter analog meters, refer to the following procedure.

5-21. Required Equipment. The following equipment is required to adjust the PA FWD PWR, PLATE E, and PLATE I digital display calibrate controls (R43, R67, R94).

A. Insulated adjustment tool, flat-tip (BE P/N 407-0083).

5-22. Procedure. To adjust the controls, proceed as follows:

NOTE ENSURE THE TRANSMITTER FORWARD POWER, PLATE VOLTAGE, AND PLATE CURRENT METERS ARE CORRECTLY CALIBRATED BEFORE PROCEEDING.
NOTE

5-23. Apply power and operate the transmitter at the normal RF power.

5-24. Observe the transmitter OUTPUT POWER meter and the PA OUTPUT value displayed on the normal display screen.

5-25. Refer to Figure 5-2 and adjust R43 until the digital value displayed on the normal display screen is equal to the indication on the meter.

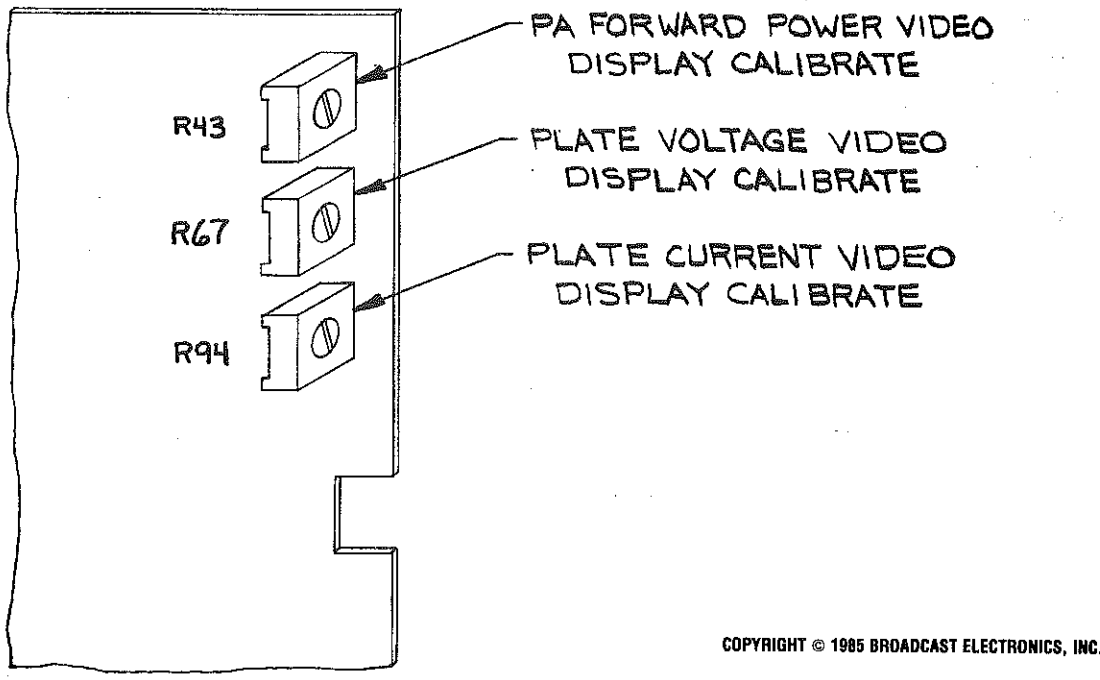
5-26. Repeat the R43 procedure for PLATE VOLTAGE and PLATE CURRENT, adjusting R67 and R94 until the value on the normal display screen is equal to the indication on the respective meter.

5-27. ANALOG/DIGITAL CONVERTER OFFSET VOLTAGE ADJUST (R85, R86, R87). Potentiometers R85, R86, and R87 adjust the analog/digital converter offset voltage. Due to the critical function of the offset voltage controls, field adjustment is not recommended. If adjustment is required, the analog/digital circuit board must be returned to the factory for calibration.

5-28. TROUBLESHOOTING.

5-29. Troubleshooting within the controller circuit board cage is not considered hazardous due to the low voltages and currents involved. All high voltages used within the controller cabinet have been shielded, however do not touch any component within the controller cabinet with power energized.

WARNING: DISCONNECT POWER PRIOR TO SERVICING



597-0036-20

FIGURE 5-2. ANALOG/DIGITAL CIRCUIT BOARD CONTROLS

5-30. If any MVDS maintenance requires removal of the controller cabinet or troubleshooting within the transmitter, refer to the applicable transmitter manual for safety and maintenance procedures. Never open the transmitter unless all primary power is disconnected.

NOTE WHEN MVDS IS DISABLED, ALL LOCAL AND REMOTE METER INDICATIONS WILL BE INACCURATE. TO CORRECT THE

NOTE METER INDICATIONS, REMOVE CABLE W7 FROM THE ANALOG-TO-DIGITAL CONVERTER CIRCUIT BOARD.

5-31. An extender circuit board with a reset switch is provided to assist troubleshooting. The reset switch clears all the digital circuitry which allows the system to generate new data. When the extender circuit board is not used, it must be inserted in the far left receptacle in the controller circuit board cage.

5-32. The troubleshooting philosophy for the MVDS consists of isolating a problem to a specific circuit board. The problem may be isolated by referencing the following warnings and Table 5-1 which lists specific symptoms and items to check.

WARNING: DISCONNECT POWER PRIOR TO SERVICING

TABLE 5-1. MVDS TROUBLESHOOTING

SYMPTOM	ITEMS TO CHECK
Missing Video Display	Power supply, video monitor, video cables W6 and W10, and the VDM circuit board.
An Entire Highlighted Screen With Missing Video Display (all green display)	Cable W11.
Flashing Video Display	CPU circuit board switch programming, microprocessor, 64K memory circuit board.
Unstable Data Values On Video Display	Cable W7, analog/digital circuit board.
Inoperative Keyboard	+5V keyboard supply at pin 11 on the EMI filter circuit board, keyboard cable, cable W8, input/output circuit board.
Disabled Logging	Correct log interface and status of logging system on the customer configuration screen, cable W8, cables to the logging devices, input/output circuit board.
Missing Clock Information After A Power Failure	Clock batteries.

WARNING

WARNING

NEVER OPEN THE TRANSMITTER UNLESS ALL POWER IS DISCONNECTED. USE THE GROUNDING STICKS PROVIDED TO ENSURE ALL COMPONENTS ARE DISCHARGED BEFORE ATTEMPTING ANY MAINTENANCE.

WARNING

REMOVE ALL JEWELRY BEFORE TROUBLESHOOTING.

WARNING

WARNING

REMOVE ALL POWER BEFORE INSERTING OR REMOVING PRINTED CIRCUIT BOARDS OR REPLACING ANY COMPONENTS.

CAUTION

CAUTION

WHEN REPLACING A COMPONENT MOUNTED ON A HEAT SINK, ENSURE A THIN FILM OF A ZINC-BASED HEAT-SINK COMPOUND IS USED (BE P/N 700-0028) TO ASSURE GOOD HEAT DISSIPATION.

CAUTION

CAUTION

INADVERTENT CONTACT BETWEEN ADJACENT COMPONENTS OR CIRCUIT BOARDS WITH TEST EQUIPMENT CAN CAUSE SERIOUS DAMAGE TO THE MVDS.

NOTE

NOTE

IF AN ANALOG/DIGITAL CONVERTER FAILS, THE ANALOG/DIGITAL CIRCUIT BOARD MUST BE RETURNED TO THE FACTORY FOR REPAIR.

5-33. Once the trouble is isolated and power is totally deenergized, it is suggested that the exact problem be located with resistance checks using the schematic diagrams and the theory of operation. The faulty component may be repaired locally or the entire device may be returned to Broadcast Electronics, Inc. for repair or replacement.

5-34. COMPONENT REPLACEMENT. Refer to Section V of the applicable transmitter manual for the component replacement procedure.

SECTION VI

PARTS LIST

6-1. INTRODUCTION.

6-2. This section provides descriptions and part numbers of parts and assemblies required for maintenance of the Broadcast Electronics MVDS. Each table entry in this section is indexed by the reference designators of the applicable schematic diagram.

6-3. Table 6-1 indexes all tables listing assemblies and sub-assemblies having replaceable parts, the table number listing the parts, and the page number of the applicable table.

TABLE 6-1. REPLACEABLE PARTS LIST INDEX

TABLE NO.	DESCRIPTION	PART NO.	PAGE
6-2	MICROPROCESSOR VIDEO DIAGNOSTICS SYSTEM OPTION	909-0091	6-2
6-3	MICROPROCESSOR MOTHERBOARD ASSEMBLY	919-0023	6-2
6-4	VIDEO DISPLAY MODULE CIRCUIT BOARD ASSEMBLY	919-0036	6-2
6-5	INPUT FILTER CIRCUIT BOARD ASSEMBLY	919-0057	6-4
6-6	ANALOG/DIGITAL CIRCUIT BOARD ASSEMBLY	919-0058/ -001	6-4
6-7	CENTRAL PROCESSOR UNIT CIRCUIT BOARD ASSEMBLY	919-0059	6-6
6-8	INPUT/OUTPUT CIRCUIT BOARD ASSEMBLY	919-0024	6-7
6-9	64K MEMORY CIRCUIT BOARD ASSEMBLY	918-0017-001/ -003/ -005/ -010/ -030/ -035	6-10
6-10	CABLE ASSEMBLY, FM MICROPROCESSOR	949-0105	6-10
6-11	CABLE ASSEMBLY, MICROPROCESSOR POWER SUPPLY	949-0035	6-11
6-12	ASSEMBLY, EXHAUST AIR TEMPERATURE SENSOR	919-0082	6-11

TABLE 6-2. MICROPROCESSOR VIDEO DIAGNOSTICS SYSTEM OPTION - 909-0091

REF. DES.	DESCRIPTION	PART NO.	QTY.
----	Fuse, AGC, 2 Ampere, Slow-Blow	334-0200	2
----	Microprocessor Motherboard Assembly	919-0023	1
----	Video Display Module Circuit Board Assembly	919-0036	1
----	Input Filter Circuit Board Assembly	919-0057	1
----	Analog/Digital Circuit Board Assembly	919-0058	1
----	Central Processor Unit Circuit Board Assembly	919-0059	1
----	Input/Output Circuit Board Assembly	919-0024	1
----	64K Memory Circuit Board Assembly	918-0017	1
----	Keyboard, Serial No: ASCII	808-4003	1
----	Assembly, Monitor	959-0135	1
----	BNC Receptacle, Bulkhead, UG492A/U	417-0017	1
----	Connector, Adaptor, BNC to UHF	417-0126	1
	Turnlock Fastener, (For Monitor Assembly)		
	Stud	420-0020	2
	Retainer Ring	420-0021	2
----	Cable Assembly, FM Microprocessor	949-0105	1
----	Cable Assembly, Microprocessor Power Supply	949-0035	1
----	Assembly, Exhaust Air Temperature Sensor	919-0082	1

TABLE 6-3. MICROPROCESSOR MOTHERBOARD ASSEMBLY - 919-0023

REF. DES.	DESCRIPTION	PART NO.	QTY.
J2 THRU J8	Connector, 100-Pin	418-5001	7
----	Connector, 6-Pin	417-0677	1
----	Blank Circuit Board	519-0023	1

TABLE 6-4. VIDEO DISPLAY MODULE CIRCUIT BOARD ASSEMBLY - 919-0036
(Sheet 1 of 3)

REF. DES.	DESCRIPTION	PART NO.	QTY.
C1 THRU C6, C9 THRU C13	Capacitor, Ceramic Monolithic, 0.1 uF ±20%, 100V	003-1054	11
C14	Capacitor, Electrolytic, 10 uF ±20%, 25V, Tantalum	063-1074	1
C15 THRU C18	Capacitor, Ceramic Monolithic, 0.1 uF ±20%, 100V	003-1054	4
C19,C20	Capacitor, Electrolytic, 10 uF ±20%, 25V, Tantalum	063-1074	2
C23	Capacitor, Ceramic Monolithic, 0.1 uF ±20%, 100V	003-1054	1
C24	Capacitor, Electrolytic, 10 uF ±20%, 25V, Tantalum	063-1074	1
C25	Capacitor, Ceramic, 10 pF ±10%, 1 kV	001-1014	1
C26	Capacitor, Mica, 1000 pF ±5%, 500W Vdc	041-1032	1
CR2	Diode, 1N4148, Silicon, 75V, 0.3 Amperes	203-4148	1
J2	Header, 3-Pin	417-0003	1
J3	Connector, BNC, 90° Angle	417-0037	1
P2	Jumper, Programmable	340-0004	1
Q1	Transistor, 2N3904, Silicon, NPN, TO-92 Case	211-3904	1
R1,R2	Resistor, 2.2 k Ohm ±5%, 1/4W	100-2243	2
R3	Resistor, 100 Ohm ±5%, 1/4W	100-1033	1
R4	Resistor, 2.2 k Ohm ±5%, 1/4W	100-2243	1
R5	Resistor, 1.5 k Ohm ±5%, 1/4W	100-1543	1
R6 THRU R8	Resistor, 560 Ohm ±5%, 1/4W	100-5633	3
R10 THRU R12	Resistor, 2.2 k Ohm ±5%, 1/4W	100-2243	3
R13	Resistor, 22 k Ohm ±5%, 1/4W	100-2253	1
R14	Resistor, 4.7 k Ohm ±5%, 1/4W	100-4743	1
R15	Resistor, 2.2 k Ohm ±5%, 1/4W	100-2243	1
RP1	Resistor Network, AB210A103, 10 k Ohm, Single-In-Line Package, 10-Pin	226-1050	1
U2	Integrated Circuit, SN74LS04N, Schottky Hex Inverter, 14-Pin DIP	228-2404	1
U3	Integrated Circuit, SN74LS86N, Quad 2-Input XOR, Schottky, 14-Pin	228-2486	1

TABLE 6-4. VIDEO DISPLAY MODULE CIRCUIT BOARD ASSEMBLY - 919-0036
(Sheet 2 of 3)

REF. DES.	DESCRIPTION	PART NO.	QTY.
U4	Integrated Circuit, SN7425N, Dual 4-Input, NOR Gate, 14-Pin DIP	228-0009	1
U6	Integrated Circuit, 74LS74N, Dual D-Type Flip-FLOP, 14-Pin	228-0074	1
U8	Integrated Circuit, SN74LS157N, Schottky Quad 2-Line to 1-Line Data Selector, 16-Pin DIP	228-0007	1
U9	Integrated Circuit, CRT5027, Timing and Control, 40-Pin DIP	228-0013	1
U10	Integrated Circuit, SN74LS157N, Schottky Quad 2-Line to 1-Line Data Selector, 16-Pin DIP	228-0007	1
U11	Integrated Circuit, Z80A, 40-Pin DIP	229-3880	1
U12	Integrated Circuit, SN74163N, 4-Bit Synchronous Counter, 16-Pin DIP	228-0011	1
U13	Integrated Circuit, SN74LS165N, Schottky 8-Bit Shift Register, 16-Pin DIP	228-0004	1
U14	Integrated Circuit, SN74S04N, Schottky Hex Inverter, 14-Pin	228-0008	1
U15	Integrated Circuit, SN74LS93N, Schottky 4-Bit Counter, 14-Pin DIP	228-0010	1
U16	Integrated Circuit, SN74LS20N, Dual 4-Input, Schottky, 14-Pin DIP	228-2420	1
U17	Integrated Circuit, SN74LS10N, 3-Input NAND Gate, Schottky, 14-Pin DIP	228-2410	1
U18	Integrated Circuit, SN74LS157N, Schottky Quad 2-Line to 1-Line Data Selector, 16-Pin DIP	228-0007	1
U19	Integrated Circuit, SN74LS368N, Hex Bus Driver Schottky, 16-Pin DIP	228-0002	1
U20	Integrated Circuit, 74LS74N, Dual D-Type Flip-Flop, 14-Pin	228-0074	1
U21	Integrated Circuit, SN74LS155N, Schottky Decoder-Demultiplexer, 16-Pin DIP	228-0006	1
U22	Integrated Circuit, SN74LS04N, Schottky Hex Inverter, 14-Pin DIP	228-2404	1
U23	Integrated Circuit, SN74LS00N, Quad NAND Gate, Schottky, 14-Pin DIP	228-2400	1
U24 THRU U27	Integrated Circuit, MM2114, 1024 X 4-Bit Static RAM, 18-Pin DIP	228-0012	4
U29	Integrated Circuit, SN74LS273N, Octal D-Type Latch, Schottky, 20-Pin DIP	228-0003	1
U30	Integrated Circuit, SN74LS373N, Octal D-Type Latch, Schottky, 20-Pin DIP	228-0001	1
U31	Integrated Circuit, SN74LS14N, Hex Schmitt-Trigger Inverter, 14-Pin DIP	228-2414	1
U32	Integrated Circuit, SN74LS20N, Dual 4-Input, Schottky, 14-Pin DIP	228-2420	1
U33	Integrated Circuit, SN74LS273N, Octal D-Type Latch, Schottky, 20-Pin DIP	228-0003	1
U34	Integrated Circuit, SN74LS157N, Schottky Quad 2-Line to 1-Line Data Selector, 16-Pin DIP	228-0007	1
U35	Integrated Circuit, SN74LS139N, Schottky Dual 2-Line to 4-Line Decoder, 16-Pin DIP	228-0005	1
U36	Integrated Circuit, SN74LS00N, Quad NAND Gate, Schottky, 14-Pin DIP	228-2400	1
VR1	Voltage Regulator, MC7812CK, 12V, 1.5 Ampere	227-7812	1
XU2 THRU XU6	Receptacle, 14-Pin DIP	417-1404	5
XU7	Receptacle, 28-Pin DIP	417-2804	1
XU8	Receptacle, 16-Pin DIP	417-1604	1
XU9	Receptacle, 40-Pin DIP	417-4005	1
XU10	Receptacle, 16-Pin DIP	417-1604	1
XU11	Receptacle, 40-Pin DIP	417-4005	1
XU12,XU13	Receptacle, 16-Pin DIP	417-1604	2
XU14 THRU XU17	Receptacle, 14-Pin DIP	417-1404	4
XU18,XU19	Receptacle, 16-Pin DIP	417-1604	2
XU20	Receptacle, 14-Pin DIP	417-1404	1
XU21	Receptacle, 16-Pin DIP	417-1604	1
XU22,XU23	Receptacle, 14-Pin DIP	417-1404	2
XU24 THRU XU27	Receptacle, 18-Pin DIP	417-1804	4

TABLE 6-4. VIDEO DISPLAY MODULE CIRCUIT BOARD ASSEMBLY - 919-0036
(Sheet 3 of 3)

REF. DES.	DESCRIPTION	PART NO.	QTY.
XU28	Receptacle, 28-Pin DIP	417-2804	1
XU29,XU30	Receptacle, 20-Pin DIP	417-2004	2
XU31,XU32	Receptacle, 14-Pin DIP	417-1404	2
XU33	Receptacle, 20-Pin DIP	417-2004	1
XU34,XU35	Receptacle, 16-Pin DIP	417-1604	2
XU36	Receptacle, 14-Pin DIP	417-1404	1
Y1	Crystal, 14.43098 MHz ±0.05% @ 20 to 50°C, AT Cut, NE18A Case	390-0005	1
----	Integrated Circuit, AM2764A-2DC, EPROM, 8K X 8, Programmed with Video Display Module Control and Character Generator Software U7 and U28, V2.0	220-2764	2
----	Blank Circuit Board	518-6351	1

TABLE 6-5. INPUT FILTER CIRCUIT BOARD ASSEMBLY - 919-0057

REF. DES.	DESCRIPTION	PART NO.	QTY.
C1 THRU C20	Capacitor, Mica, 390 pF ±5%, 100V	042-3922	20
C21	Capacitor, Electrolytic, 10 uF, 35V	023-1076	1
C22 THRU C28	Capacitor, Mica, 390 pF ±5%, 100V	042-3922	7
C29	Capacitor, Mylar Film, 0.1 uF, 100V	030-1053	1
C30 THRU C60	Capacitor, Mica, 390 pF ±5%, 100V	042-3922	31
D1	Diode, 1N4005, Silicon, 600V @ 1 Ampere	203-4005	1
J1 THRU J4	Connector, 25-Pin	417-2500	4
L1 THRU L28	Choke, RF: 4.7 uH, 430 mA DC Resistance: 0.55 Ohms Resonant Frequency: 115 MHz	360-0022	28
----	Integrated Circuit, MC1805CT, Voltage Regulator, 5V @ 1.0 Ampere, TO-220 Case	227-7805	1
----	Header, 2-Pin, 90° Angle	417-0075	1
----	Plug, Keying AMP 206509-1	417-0090	4
----	Blank Circuit Board	519-0057	1

TABLE 6-6. ANALOG/DIGITAL CIRCUIT BOARD ASSEMBLY - FM-1.5A, FM-3.5A, FM-5A, FM-10A - 919-0058, FM-30A, FM-35A - 919-0058-001 (Sheet 1 of 3)

REF. DES.	DESCRIPTION	PART NO.	QTY.
C1 THRU C16	Capacitor, Electrolytic, 10 uF, 35V	023-1076	16
C24	Capacitor, Mylar Film, .01 uF ±10%, 100V	031-1043	1
C25	Capacitor, Electrolytic, 100 uF ±10%, 16V	020-1082	1
C26 THRU C28	Capacitor, Electrolytic, 4.7 uF, 35V	024-4764	3
C29 THRU C39	Capacitor, Mylar Film, .01 uF ±10%, 100V	031-1043	11
C45	Capacitor, Electrolytic, 47 uF, 35V	020-4770	1
C46	Capacitor, Electrolytic, 100 uF ±10%, 16V	020-1082	1
C47	Capacitor, Electrolytic, 47 uF, 35V	020-4770	1
C48 THRU C56	Capacitor, Mylar Film, .01 uF ±10%, 100V	031-1043	9
D1 THRU D16, D24 THRU D39	Diode, 1N4005, Silicon, 600V, 1 Ampere	203-4005	32
J2,J3,J6 THRU J9	Header, 3-Pin	417-0003	6
P2,P3,P6 THRU P9	Jumper, Programmable	340-0004	6
Q1	Transistor, 2N3904, Silicon, NPN, TO-92 Case	211-3904	1
R1 THRU R16	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	16
R24	Resistor, 1.21 k Ohm ±1%, 1/4W	103-1214	1
R25,R26	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	2

TABLE 6-6. ANALOG/DIGITAL CIRCUIT BOARD ASSEMBLY - FM-1.5A, FM-3.5A, FM-5A, FM-10A - 919-0058, FM-30A, FM-35A - 919-0058-001 (Sheet 2 of 3)

REF. DES.	DESCRIPTION	PART NO.	QTY.
R27	Resistor, 23.2 k Ohm ±1%, 1/4W	103-2325	1
R31	Resistor, 8.66 k Ohm ±1%, 1/4W	100-8641	1
R32 THRU R34	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	3
R35	Resistor, 1 Meg Ohm ±1%, 1/4W	103-1007	1
R36	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	1
R37	Resistor, 210 k Ohm ±1%, 1/4W	103-2106	1
R41	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	1
R42	Resistor, 4.99 k Ohm ±1%, 1/4W	100-5041	1
R43	Potentiometer, 2 k Ohm ±10%, 1/2W	178-2044	1
R44	Resistor, 97.6 k Ohm ±1%, 1/4W	100-9751	1
R45,R46, R48,R53	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	4
R54	Resistor, 9.09 k Ohm ±1%, 1/4W	103-9041	1
R55	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	1
R56	Resistor, 8.25 k Ohm ±1%, 1/4W	103-8254	1
R57,R58, R60 THRU R62	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	5
R67	Potentiometer, 1 k Ohm ±10%, 1/2W	178-1043	1
R68	Resistor, 9.31 k Ohm ±1%, 1/4W	103-9314	1
R69	Resistor, 6650 Ohm ±1%, 1/4W	103-6641	1
R70	Resistor, 9.09 k Ohm ±1%, 1/4W	103-9041	1
R71	Resistor, 6650 Ohm ±1%, 1/4W	103-6641	1
R72	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	1
R74	Resistor, 4.7 k Ohm ±5%, 1/4W	100-4743	1
R75	Resistor, 130 k Ohm ±1%, 1/4W	103-1306	1
R77	Resistor, 100 k Ohm ±1%, 1/4W	103-1062	1
R78	Resistor, 20 k Ohm ±1%, 1/4W	103-2051	1
R79	Resistor, 8.25 k Ohm ±1%, 1/4W	103-8254	1
R80,R81	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	2
R82	Resistor, 8.25 k Ohm ±1%, 1/4W	103-8254	1
R84	Resistor, 4.7 k Ohm ±5%, 1/4W	100-4743	1
R85,R86	Potentiometer, 100 Ohm ±10%, 1/2W	177-1034	2
R88	Resistor, 220 k Ohm ±5%, 1/4W	100-2263	1
R89	Resistor, 20 k Ohm ±1%, 1/4W	103-2051	1
R90	Resistor, 100 k Ohm ±1%, 1/4W	103-1062	1
R91	Resistor, 4.7 k Ohm ±5%, 1/4W	100-4743	1
R92	Resistor, 100 Ohm ±5%, 1/4W	100-1033	1
R93	Resistor, 10 k Ohm ±5%, 1/4W	100-1053	1
R95,R96	Resistor, 1 Meg Ohm ±1%, 1/4W	103-1007	2
U1 THRU U10,U14	Integrated Circuit, TL072CP, Dual Operational Amplifier, 8-Pin DIP	221-0072	11
U16	Integrated Circuit, AD581KH, Negative 10V Precision Regulator, TO-5 Case	220-0581	1
U17	Integrated Circuit, SN74LS04N, Low-Power Schottky Hex Inverter, 14-Pin DIP	228-2404	1
U18	Integrated Circuit, SN74LS00N, Low-Power Quad NAND Gate, 14-Pin DIP	228-2400	1
U19	Integrated Circuit, SN74LS20N, Schottky Dual 4-Input NAND Gate, 14-Pin DIP	228-2420	1
U20	Integrated Circuit, SN74LS30N, Schottky 8-Input NAND Gate, 14-Pin DIP	228-2430	1
U21,U22	Integrated Circuit, SN74LS244N, Octal Tri-State Bus Driver, 20-Pin DIP	228-2244	2
U23	Integrated Circuit, SN74LS42N, BCD-To-Decimal Decoder, 16-Pin DIP	228-2442	1
U24	Integrated Circuit, 74LS74N, Dual D-Type Flip-Flop, 14-Pin DIP	228-0074	1
U25	Integrated Circuit, 74LS123, Schottky Dual Monostable Multivibrator, 16-Pin DIP	220-2123	1
U26,U27	Integrated Circuit, AD7581LN, 8-Channel A-D Converter, CMOS, 28-Pin DIP	220-7581	2
XU1 THRU XU10,XU14	Socket, 8-Pin DIP	417-0804	11
XU17 THRU XU20	Socket, 14-Pin DIP	417-1404	4
XU21,XU22	Socket, 20-Pin DIP	417-2004	2
XU23	Socket, 16-Pin DIP	417-1604	1

TABLE 6-6. ANALOG/DIGITAL CIRCUIT BOARD ASSEMBLY - FM-1.5A, FM-3.5A, FM-5A, FM-10A - 919-0058, FM-30A, FM-35A - 919-0058-001 (Sheet 3 of 3)

REF. DES.	DESCRIPTION	PART NO.	QTY.
XU24	Socket, 14-Pin DIP	417-1404	1
XU25	Socket, 16-Pin DIP	417-1604	1
XU26,XU27	Socket, 28-Pin DIP	417-2804	2
----	Pad, Transistor Mounting, TO-18 Case	409-0121	1
----	Blank Circuit Board	519-0058	1
	ADDITIONAL PARTS FOR ANALOG/DIGITAL CIRCUIT BOARD ASSEMBLY - 919-0058		
R47	Resistor, 12.7 k Ohm ±1%, 1/4W	103-1275	1
R59	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	1
R73	Resistor, 12.7 k Ohm ±1%, 1/4W	103-1275	1
R76	Resistor, 20 k Ohm ±1%, 1/4W	103-2051	1
R94	Potentiometer, 5 k Ohm ±10%, 1/2W	178-5043	1
	ADDITIONAL PARTS FOR ANALOG/DIGITAL CIRCUIT BOARD ASSEMBLY - 919-0058-001		
C17 THRU C23	Capacitor, Electrolytic, 10 uF, 35V	023-1076	7
C40 THRU C44	Capacitor, Mylar, 0.01 uF ±10%, 100V	031-1043	5
D17 THRU D23, D40 THRU D46	Diode, 1N4005, Silicon, 600V @ 1 Ampere	203-4005	14
J4	Header, 3-Pin	417-0003	1
P4	Jumper, Programmable	340-0004	1
R17 THRU R23, R28 THRU R30, R38 THRU R40	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	13
R47	Resistor, 12.7 k Ohm ±1%, 1/4W	103-1275	1
R49 THRU R52	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	4
R59	Resistor, 24.9 k Ohm ±1%, 1/4W	103-2495	1
R63 THRU R66	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	4
R73	Resistor, 12.7 k Ohm ±1%, 1/4W	103-1275	1
R76	Resistor, 40.2 k Ohm ±1%, 1/4W	103-4025	1
R83	Resistor, 8.25 k Ohm ±1%, 1/4W	103-8254	1
R87	Potentiometer, 100 Ohm ±10%, 1/2W	177-1034	1
R94	Potentiometer, 10 k Ohm ±10%, 1/2W	178-1054	1
U11 THRU U13, U15	Integrated Circuit, TL072CP, Dual Operational Amplifier, 8-Pin DIP	221-0072	4
U28	Integrated Circuit, AD7581LN, 8-Channel A-D Converter, CMOS, 28-Pin DIP	220-7581	1
XU11 THRU XU13, XU15	Socket, 8-Pin DIP	417-0804	4
XU28	Socket, 28-Pin DIP	417-2804	1

TABLE 6-7. CENTRAL PROCESSOR UNIT CIRCUIT BOARD ASSEMBLY - 919-0059 (Sheet 1 of 2)

REF. DES.	DESCRIPTION	PART NO.	QTY.
C1	Capacitor, Ceramic Disc, 10 pF ±10%, 1 kV	001-1014	1
C2	Capacitor, Mica, 1000 pF ±5%, 500V	041-1032	1
C3,C4	Capacitor, Electrolytic, 100 uF, 40V	014-1084	2
C5 THRU C22	Capacitor, Ceramic, 0.1 uF +80 -20, 10V	000-1055	18
D1	Diode, 1N4148, Silicon, 75V, 0.3 Ampere	203-4148	1
R1,R2	Resistor, 560 Ohm ±5%, 1/4W	100-5633	2
R3	Resistor, 22 k Ohm ±5%, 1/4W	100-2253	1
R4	Resistor, 100 Ohm ±5%, 1/4W	100-1033	1
R5,R14,R23	Resistor Network, AB210A103, 10 k Ohm, Single-In-Line Package, 10-Pin	226-1050	3

TABLE 6-7. CENTRAL PROCESSOR UNIT CIRCUIT BOARD ASSEMBLY - 919-0059
(Sheet 2 of 2)

REF. DES.	DESCRIPTION	PART NO.	QTY.
R32 THRU R34	Resistor, 1 k Ohm ±5%, 1/4W	100-1043	3
S1	Switch Assembly, SPST, 8-Position DIP	340-0003	1
U1,U2	Integrated Circuit, SN74LS175N, Hex/Quad, Flip-Flop, 16-Pin DIP	228-2175	2
U3	Integrated Circuit, SN74LS00N, Quad NAND Gate, 14-Pin DIP	228-2400	1
U4	Integrated Circuit, SN74LS175N, Hex/Quad, Fkip-Flop, 16-Pin DIP	228-2175	1
U5	Integrated Circuit, SN74LS04N, Hex Inverter, 14-Pin DIP	228-2404	1
U6	Integrated Circuit, SN74LS00N, Quad NAND Gate, 14-Pin DIP	228-2400	1
U7	Integrated Circuit, SN74LS02N, Quad NOR Gate, 14-Pin DIP	228-2402	1
U8	Integrated Circuit, SN74LS04N, Hex Inverter, 14-Pin DIP	228-2404	1
U9	Integrated Circuit, SN74LS244, Octal Tri-State Bus Driver, 20-Pin	228-2244	1
U10	Integrated Circuit, SN74LS02N, Quad NOR Gate, 14-Pin DIP	228-2402	1
U11	Integrated Circuit, SN74LS244, Octal Tri-State Bus Driver,	228-2244	1
U12	Integrated Circuit, Z-80A, Central Processor Unit, 40-Pin DIP	229-3880	1
U13	Integrated Circuit, SN74LS175N, Hex/Quad, Flip-Flop, 16-Pin DIP	228-2175	1
U14	Integrated Circuit, SN74LS258, Quad 2-Input Multiplexer with Inverted Tri-State Outputs, 16-Pin	228-2258	1
U15	Integrated Circuit, SN74LS14N, Hex Schottky Schmitt-Trigger Inverter, 14-Pin DIP	228-2414	1
U16 THRU U20	Integrated Circuit, SN74LS244, Octal Tri-State Bus Driver, 20-Pin	228-2244	5
U21	Integrated Circuit, SN74LS258, Quad 2-Input Multiplexer with Inverted Tri-State Outputs, 16-Pin	228-2258	1
XU1,XU2	Receptacle, 16-Pin DIP	417-1604	2
XU3	Receptacle, 14-Pin DIP	417-1404	1
XU4	Receptacle, 16-Pin DIP	417-1604	1
XU5 THRU XU8	Receptacle, 14-Pin DIP	417-1404	4
XU9	Receptacle, 20-Pin DIP	417-2004	1
XU10	Receptacle, 14-Pin DIP	417-1404	1
XU11	Receptacle, 20-Pin DIP	417-2004	1
XU12	Receptacle, 40-Pin DIP	417-4005	1
XU13,XU14	Receptacle, 16-Pin DIP	417-1604	2
XU15	Receptacle, 14-Pin DIP	417-1404	1
XU16 THRU XU20	Receptacle, 20-Pin DIP	417-2004	5
XU21	Receptacle, 16-Pin DIP	417-1604	1
Y1	Crystal, 8 MHz ±0.05% from +20°C to +50°C, A/T Cut, NE18A Case	390-0018	1
----	Blank Circuit Board	514-6300	1

TABLE 6-8. INPUT/OUTPUT CIRCUIT BOARD ASSEMBLY - 919-0024
(Sheet 1 of 3)

REF. DES.	DESCRIPTION	PART NO.	QTY.
BAT1 THRU BAT3	Battery, Silver Oxide, 1.5V	350-0004	3
C1	Capacitor, Ceramic, 0.1 uF ±20%, 50V	003-1054	1
C2	Capacitor, Ceramic, Adjustable 8-25 pF, 250 Vdc	909-0825	1
C3 THRU C6	Capacitor, Ceramic, 0.1 uF ±20%, 50V	003-1054	4
C7	Capacitor, Ceramic Monolithic, 10 pF ±5%, 100V	000-1013	1
C8 THRU C31	Capacitor, Ceramic, 0.1 uF ±20%, 50V	003-1054	24
C32	Capacitor, Tantalum, 47 uF ±20%, 6V	061-4774	1
C33	Capacitor, Electrolytic, 100 uF, 16V	020-1084	1
C34,C35	Capacitor, Ceramic, 0.1 uF ±20%, 50V	003-1054	2
C36,C37	Capacitor, Ceramic Monolithic, 56 pF ±10%, 200V	001-5613	2
C38 THRU C48	Capacitor, Ceramic, 0.1 uF ±20%, 50V	003-1054	11
C49	Capacitor, Electrolytic, 10 uF, 35V	023-1076	1
C50	Capacitor, Electrolytic, 1 uF, 50V	024-1064	1

TABLE 6-8. INPUT/OUTPUT CIRCUIT BOARD ASSEMBLY - 919-0024
(Sheet 2 of 3)

REF. DES.	DESCRIPTION	PART NO.	QTY.
C51	Capacitor, Ceramic Disc, 100 pF, 100V	002-1024	1
D1 THRU D13	Diode, 1N4148, Silicon, Signal Switching, 75V @ 300 mA Maximum	203-4148	13
J5 THRU J7	Header, 3-Pin	417-0003	3
P4	Socket, 16-Pin	417-1604	1
P5 THRU P7	Jumper, Programmable	340-0004	3
Q1 THRU Q7	Transistor, 2N3904, Silicon, NPN, TO-92 Case	211-3904	7
R1 THRU R3	Resistor, 10 k Ohm ±5%, 1/4W	100-1053	3
R4 THRU R10	Resistor, 4.7 k Ohm ±5%, 1/4W	100-4743	7
R11	Resistor, 330 k Ohm ±5%, 1/4W	100-3363	1
R12,R13	Resistor, 10 Meg Ohm ±5%, 1/4W	100-1083	2
R14,R15	Resistor, 1 k Ohm ±5%, 1/4W	100-1043	2
R17	Resistor, 4.7 k Ohm ±5%, 1/4W	100-4743	1
R18	Resistor, 10 k Ohm ±5%, 1/4W	100-1053	1
R19 THRU R23	Resistor, 4.7 k Ohm ±5%, 1/4W	100-4743	5
R24	Resistor, 68 k Ohm ±5%, 1/4W	100-6853	1
R25 THRU R27	Resistor, 4.7 k Ohm ±5%, 1/4W	100-4743	3
R28	Resistor, 100 k Ohm ±5%, 1/4W	100-1063	1
R29	Resistor, 10 k Ohm ±5%, 1/4W	100-1053	1
R30	Resistor, 10 Meg Ohm ±5%, 1/4W	100-1083	1
R31	Resistor, 470 k Ohm ±5%, 1/4W	100-4763	1
R32,R33	Resistor, 100 Ohm ±5%, 1/4W	100-1033	2
R34	Resistor, 4.7 k Ohm ±5%, 1/4W	100-4743	1
R35	Resistor, 2.2 k Ohm ±5%, 1/4W	100-2243	1
RN1 THRU RN3	Resistor Network, 8-22 k Ohm 1/4W Resistors, 16-Pin DIP	226-2250	3
RN4 THRU RN6	Resistor Network, AB210A103, 10 k Ohm, Single-In-Line Package, 10-Pin	226-1050	3
RN7	Resistor Network, 8-22 k Ohm 1/4W Resistors, 16-Pin DIP	226-2250	1
RN8	Resistor Network, AB210A103, 10 k Ohm, Single-In-Line Package, 10-Pin	226-1050	1
RN9	Resistor Network, 8-22 k Ohm 1/4W Resistors, 16-Pin DIP	226-2250	1
RN10	Resistor Network, AB210A103, 10 k Ohm, Single-In-Line Package, 10-Pin	226-1050	1
RN11	Resistor Network, AB410A471, 9-470 Ohm 1/4W Resistors, Single-In-Line Package, 10-Pin	226-0470	1
S1	Switch, 4-SPST, Side Adjust, 8-Pin DIP	340-0013	1
S2 THRU S4	Switch, 8-SPST, 16-Pin DIP	340-0003	3
U1	Integrated Circuit, 8255A, Programmable Peripheral Interface, 24 Parallel Input/Output Lines, 40-Pin DIP	229-8255	1
U2,U3	Integrated Circuit, 14505, Hex Level Shifter, TTL to CMOS, 16-Pin DIP	228-4504	2
U4	Integrated Circuit, CD4069CN, Hex Inverter, CMOS, 14-Pin DIP	228-4069	1
U5,U6	Integrated Circuit, 14505, Hex Level Shifter, TTL to CMOS, 16-Pin DIP	228-4504	2
U7 THRU U9	Integrated Circuit, 8255A, Programmable Peripheral Interface, 24 Parallel Input/Output Lines, 40-Pin DIP	229-8255	3
U10	Integrated Circuit, SN7475N, 4-Bit Bistable Latch, 16-Pin DIP	228-7475	1
U11 THRU U13	Integrated Circuit, 8251A, Universal Synchronous/Asynchronous Receiver/Transmitter (USART), NMOS, 28-Pin DIP	229-8251	3
U14 THRU U16	Integrated Circuit, RC741DN, Operational Amplifier, 8-Pin DIP	221-7410	3
U17	Integrated Circuit, SN74LS164N, 8-Bit Parallel Output Shift Register, TTL, 14-Pin DIP	228-2164	1
U18	Integrated Circuit, SN7475N, 4-Bit Bistable Latch, 16-Pin DIP	228-7475	1
U19	Integrated Circuit, SN74LS00N, Schottky Quad NAND Gate, 14-Pin DIP	228-2400	1
U20	Integrated Circuit, SN74LS42N, Dual D-Type Flip-Flop, 14-Pin DIP	228-2442	1
U21	Integrated Circuit, SN74LS123, Schottky Dual Monostable Multivibrator, 16-Pin DIP	220-2123	1
U22	Integrated Circuit, MC146818, Real Time Clock-RAM-Interface, CMOS, 24-Pin DIP	229-6818	1
U23	Integrated Circuit, 74LS04N, Low-Power Schottky Hex Inverter, 14-Pin DIP	228-2404	1

TABLE 6-8. INPUT/OUTPUT CIRCUIT BOARD ASSEMBLY - 919-0024
(Sheet 3 of 3)

REF. DES.	DESCRIPTION	PART NO.	QTY.
U24	Integrated Circuit, F4702PC, Bit Rate Generator, CMOS, 16-Pin DIP	228-8702	1
U25	Integrated Circuit, 93L34PC, 8-Bit Addressable Latch, 16-Pin DIP	228-1034	1
U26	Integrated Circuit, SN74LS164N, 8-Bit Parallel Output Shift Register, TTL, 14-Pin DIP	228-2164	1
U27	Integrated Circuit, SN74LS04N, Low-Power Schottky Hex Inverter, 14-Pin DIP	228-2404	1
U28	Integrated Circuit, SN74LS20N, Schottky Dual 4-Input NAND Gate, 14-Pin DIP	228-2420	1
U29	Integrated Circuit, SN74LS03N, Schottky NAND Gate with Open Collectors, 14-Pin DIP	228-2403	1
U30	Integrated Circuit, SN74LS10N, Schottky Triple 3-Input NAND Gate, 14-Pin DIP	228-2410	1
U31	Integrated Circuit, SN74LS14N, Schottky Hex Schmitt Trigger, 14-Pin DIP	228-2414	1
U32	Integrated Circuit, SN74LS244N, Octal Tri-State Bus Driver, 20-Pin DIP	228-2244	1
U33	Integrated Circuit, SN74LS30N, Schottky 8-Input NAND Gate, TTL, 14-Pin DIP	228-2430	1
U34,U35	Integrated Circuit, SN74LS244N, Octal Tri-State Bus Driver, 20-Pin DIP	228-2244	1
XBAT1 THRU XBAT3	Battery Holder, Button Type	350-0003	3
XU1	Socket, 40-Pin DIP	417-4005	1
XU2,XU3	Socket, 16-Pin DIP	417-1604	2
XU4	Socket, 14-Pin DIP	417-1404	1
XU5,XU6	Socket, 16-Pin DIP	417-1604	2
XU7 THRU XU9	Socket, 40-Pin DIP	417-4005	3
XU10	Socket, 16-Pin DIP	417-1604	1
XU11 THRU XU13	Socket, 28-Pin	417-2804	3
XU14 THRU XU16	Socket, 8-Pin DIP	417-0804	3
XU17	Socket, 14-Pin DIP	417-1404	1
XU18	Socket, 16-Pin DIP	417-1604	1
XU19	Socket, 14-Pin DIP	417-1404	1
XU20,XU21	Socket, 16-Pin DIP	417-1604	2
XU22	Socket, 24-Pin DIP	417-2404	1
XU23	Socket, 14-Pin DIP	417-1404	1
XU24,XU25	Socket, 16-Pin DIP	417-1604	2
XU26 THRU XU31	Socket, 14-Pin DIP	417-1404	6
XU32	Socket, 20-Pin DIP	417-2004	1
XU33	Socket, 14-Pin DIP	417-1404	1
XU34,XU35	Socket, 20-Pin DIP	417-2004	2
Y1	Oscillator, Crystal, NTF3238C, 10.5 pF, 32.768 kHz	390-0011	1
Y2	Oscillator, Integrated Circuit, CO-238T, Turntable 10 MHz, 14-Pin DIP	390-0002	1
----	Resistor, 2.2 k Ohm ±5%, 1/4W	100-2243	1
----	Blank Circuit Board	519-0024	1

TABLE 6-9. 64K MEMORY CIRCUIT BOARD ASSEMBLY - FM-1.5A - 918-0017-001, FM-3.5A - 918-0017-003, FM-5A - 918-0017-005, FM-10A - 918-0017-010, FM-30A - 918-0017-030, FM-35A - 918-0017-035

REF. DES.	DESCRIPTION	PART NO.	QTY.
C1 THRU C3	Capacitor, Ceramic, 0.01 uF ±20%, 25V	000-1044	3
C4	Capacitor, Tantalum, 1 uF ±10%, 35V	064-1063	1
C8 THRU C28	Capacitor, Ceramic, 0.01 uF ±20%, 25V	000-1044	21
J1 THRU J24	Jumper, Programmable	340-0004	24
S2	Switch, 8-SPST, 16-Pin DIP	340-0003	1
U1	Resistor Network, 410A472, 4.7 k Ohm, Single-In-Line Package, 10-Pin	226-4740	1
U2	Integrated Circuit, SN74LS138N, 1 of 8 Decoder, 16-Pin DIP	228-2138	1
U3	Resistor Network, 410A472, 4.7 k Ohm, Single-In-Line Package, 10-Pin	226-4740	1
U4	Integrated Circuit, SN74LS138N, 1 of 8 Decoder, 16-Pin DIP	228-2138	1
U5	Resistor Network, 410A472, 4.7 k Ohm, Single-In-Line Package, 10-Pin	226-4740	1
U6,U7	Integrated Circuit, SN74LS138N, 1 of 8 Decoder, 16-Pin DIP	228-2138	2
U10	Resistor Network, 783-1-R4.7K, 4.7 k Ohm, Single-In-Line Package, 6-Pin	226-4741	1
U14 THRU U17	Integrated Circuit, SN74LS244N, Octal Tri-State Bus Driver, 20-Pin DIP	228-2244	4
U18	Integrated Circuit, SN74LS266N, Quad Exclusive 2-Input NOR Gate, 14-Pin DIP	228-2266	1
U19	Resistor Network, 410A472, 4.7 k Ohm, Single-In-Line Package, 10-Pin	226-4740	1
U20	Integrated Circuit, SN74LS20N, Schottky Dual 4-Input NAND Gate, 14-Pin DIP	228-2420	1
U21	Integrated Circuit, SN74LS04N, Low-Power Schottky Hex Inverter, 14-Pin DIP	228-2404	1
U22	Integrated Circuit, SN74LS00N, Schottky Quad NAND Gate, 14-Pin DIP	228-2400	1
X1	Integrated Circuit, HM6116P-4, 2K X 8 RAM, CMOS, 24-Pin DIP	229-6116	1
X8	Integrated Circuit, MK48Z02B-25, EEPROM 2K X 8, CMOS, 24-Pin DIP	220-2816	1
X9 THRU X27,X29,X30	Integrated Circuit, MM2716Q, EPROM, NMOS, 24-Pin DIP	229-2716	21
X1 THRU X32	Socket, 24-Pin DIP	417-2404	32
----	Header, 3-Pin	417-0003	24
----	Socket, 14-Pin DIP	417-1404	4
----	Socket, 16-Pin DIP	417-1604	4
----	Socket, 20-Pin DIP	417-2004	4
----	Blank Circuit Board	518-0017	1
	ADDITIONAL PARTS FOR 64K MEMORY CIRCUIT BOARD ASSEMBLY - 918-0017-030, 918-0017-035		
X31	Integrated Circuit, MM2716Q, EPROM, NMOS, 24-Pin DIP	229-2716	1

TABLE 6-10. CABLE ASSEMBLY, FM MICROPROCESSOR - 949-0105

REF. DES.	DESCRIPTION	PART NO.	QTY.
----	Blower, 29 Ft^3/Min (0.82 m^3/Min) @ 2700 r/Min Motor: 115V, 50/60 Hz	380-0018	1
----	Interconnecting Cables:	949-0105	
W6	Video Circuit Board to Bulkhead Tee		1
W7	Controller Filter Circuit Board to Analog/Digital Circuit Board		1
W8	Microprocessor Filter Circuit Board to Input/Output Circuit Board		1
W9	Controller Filter Circuit Board to Input/Output Circuit Board		1
W10	Bulkhead Tee to Monitor		1
W11	Controller Circuit Board to Input/Output Circuit Board		1
W12	RCA Keyboard to Controller		1
W13	Assembly, Blower Cable		1

TABLE 6-11. CABLE ASSEMBLY, MICROPROCESSOR POWER SUPPLY - 949-0035

REF. DES.	DESCRIPTION	PART NO.	QTY.
J2	Connector, 6-Pin	418-0006	1
P1,P2	Connector, 6-Pin	418-0670	2
P3	Socket, 3-Contact (Line Cord Socket)	417-0107	1
P8	Connector, 2-Pin	417-0499	1
S1	Switch, Toggle, 3PDT, 5A @ 120V ac or 28V dc, 2A @ 250V ac (MVDS Power Switch)	340-0062	1
----	Pins for J2	417-0036	5
----	Pins for P1 and P2	417-0053	8
----	Pins for P8	417-8766	2
----	Power Supply MVDS System, HCAA-60W-A: AC Input: 200/120/220/230-240 Vac, 47-63 Hz DC Output: +5V @ 6A, +15V @ 1A, -15V @ 1A	540-0001	1

TABLE 6-12. ASSEMBLY, EXHAUST AIR TEMPERATURE SENSOR - 919-0082

REF. DES.	DESCRIPTION	PART NO.	QTY.
C1,C2	Capacitor, Mica, 390 pF ±5%, 100V	042-3922	2
C3,C4	Capacitor, Ceramic, .001 uF ±10%, 1 kV	002-1034	2
J1	Socket, 4-Pin	418-0255	1
R1	Resistor, 10 k Ohm ±5%, 1/4W	100-1053	1
R2	Resistor, 2.2 k Ohm ±5%, 1/4W	100-2243	1
U1	Integrated Circuit, LM35DZ, Celsius Temperature Sensor, TO-92 Case	220-0035	1
----	Blank Circuit Board	519-0082	1

SECTION VII

MVDS DRAWINGS

7-1. INTRODUCTION.

7-2. This section provides assembly drawings, schematic diagrams, and cable diagrams as indexed below for the Broadcast Electronics MVDS.

FIGURE	TITLE	NUMBER
7-1	SCHEMATIC DIAGRAM, 64K MEMORY CIRCUIT BOARD	SD908-0017
7-2	ASSEMBLY DIAGRAM, 64K MEMORY CIRCUIT BOARD	AC918-0017
7-3	SCHEMATIC DIAGRAM, ANALOG/DIGITAL CIRCUIT BOARD	SD919-0058
7-4	ASSEMBLY DIAGRAM, ANALOG/DIGITAL CIRCUIT BOARD	AD919-0058
7-5	COMPONENT LOCATOR, ANALOG/DIGITAL CIRCUIT BOARD	597-0036-21
7-6	SCHEMATIC DIAGRAM, INPUT/OUTPUT CIRCUIT BOARD	SD919-0024
7-7	ASSEMBLY DIAGRAM, INPUT/OUTPUT CIRCUIT BOARD	AD919-0024
7-8	COMPONENT LOCATOR, INPUT/OUTPUT CIRCUIT BOARD	597-0036-22
7-9	SCHEMATIC DIAGRAM, CPU CIRCUIT BOARD	SD919-0059
7-10	ASSEMBLY DIAGRAM, CPU CIRCUIT BOARD	AD919-0059
7-11	SCHEMATIC DIAGRAM, VDM CIRCUIT BOARD	SD919-0036
7-12	ASSEMBLY DIAGRAM, VDM CIRCUIT BOARD	AD919-0036
7-13	SCHEMATIC DIAGRAM, EMI FILTER CIRCUIT BOARD	SC919-0057
7-14	ASSEMBLY DIAGRAM, EMI FILTER CIRCUIT BOARD	AC919-0057
7-15	SCHEMATIC DIAGRAM, EXHAUST AIR TEMPERATURE SENSOR CIRCUIT BOARD	SB919-0082
7-16	ASSEMBLY DIAGRAM, EXHAUST AIR TEMPERATURE SENSOR CIRCUIT BOARD	AB919-0082
7-17	SCHEMATIC AND WIRING DIAGRAM, POWER SUPPLY	597-0036-23 597-0036-23A
7-18	ASSEMBLY DIAGRAM, MOTHERBOARD	AC919-0023
7-19	ASSEMBLY DIAGRAM, CONTROLLER CABINET RIBBON CABLES	597-0036-24
7-20	CABLE DIAGRAM, PARALLEL LOG PRINTER	AC949-0110

U114 74LS244

U115 74LS244

U116 74LS244

U117 74LS244

U12 74LS138

U4 74LS138

U6 74LS138

U7 74LS138

PULL-UPS ON ALL OUTPUTS OF U12

PULL-UPS ON ALL OUTPUTS OF U14

PULL-UPS ON ALL OUTPUTS OF U16 & U17

TO ALL SOCKETS X1 THRU X32 PIN NUMBERS INDICATED

TO ALL SOCKETS X1 THRU X32 PIN NUMBERS INDICATED

TO PIN 21 OF X9 THRU X32. (1 JUMPER PER SOCKET)

COMPONENTS WITHIN BROKEN LINE AREA NOT INCLUDED ON PCB

COMPONENTS WITHIN BROKEN LINE AREA NOT INCLUDED ON PCB

NOTES:
1.) SEE ASSY. #C918-0017
2.) SEE S/M # 918-0017
3.) 1 PU INDICATE A PULL UP RESISTOR, 4.7K TO +5V.
4.) (N) INDICATES PIN NUMBER 'N' ON THE PCB EDGE CONNECTOR.

TOLERANCE UNLESS OTHERWISE SPECIFIED
DECIMAL 2 PL= ±1 3PL= .005
FRACTIONAL ±1/64
ANGULAR ± 1°
SHARP EDGES TO BEND RADII
FILLET RADII

MATERIAL

TREATMENT OR FINISH

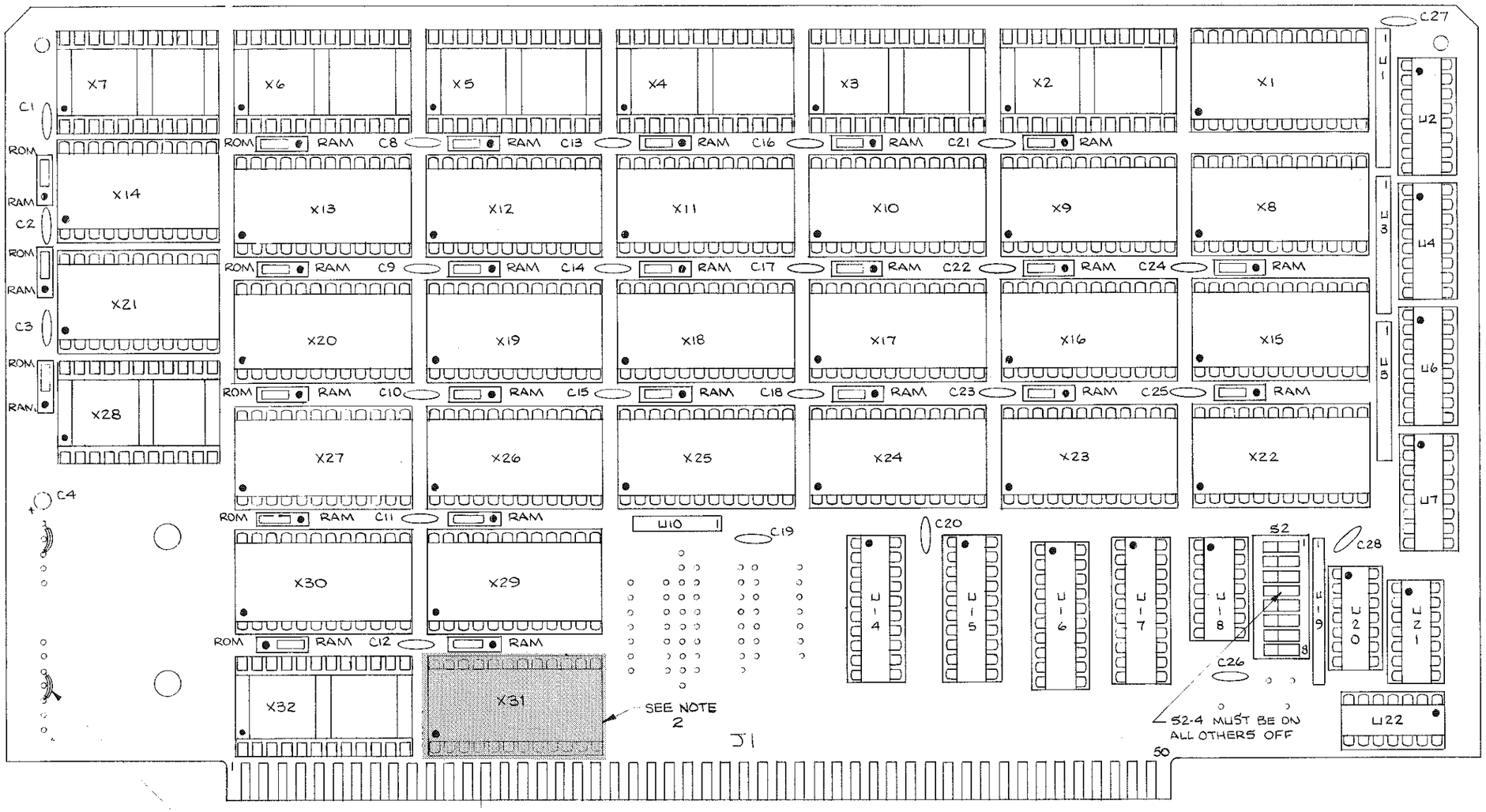
DRAWN BY DAF DATE 11-4-82
CHECKED BY DATE
PROJECT ENGR. DATE 11-8-82
APPROVED BY MH 11-8-82

BROADCAST ELECTRONICS INC.
—A FILMWAYS COMPANY—

TITLE SCHEMATIC 64K MEMORY BOARD

D DWG. NO. 908-0017 REV. A

SCALE NTS SHEET 1 OF 1



SEE SCHEMATIC # D908-0017

601-0022 BUSS WIRE
693-0220 TEFLON TUBING
(2 PLCS)

NOTE:

1. 2716BDC EPROM'S (X29, X30) ARE TO BE PROGRAMMED FOR 1.5A.
2. SOCKET X31, INDICATED BY SHADED AREA, TO BE FILLED WITH PROGRAMMED EPROM FOR 919-0202 BOARDS ONLY.

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TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

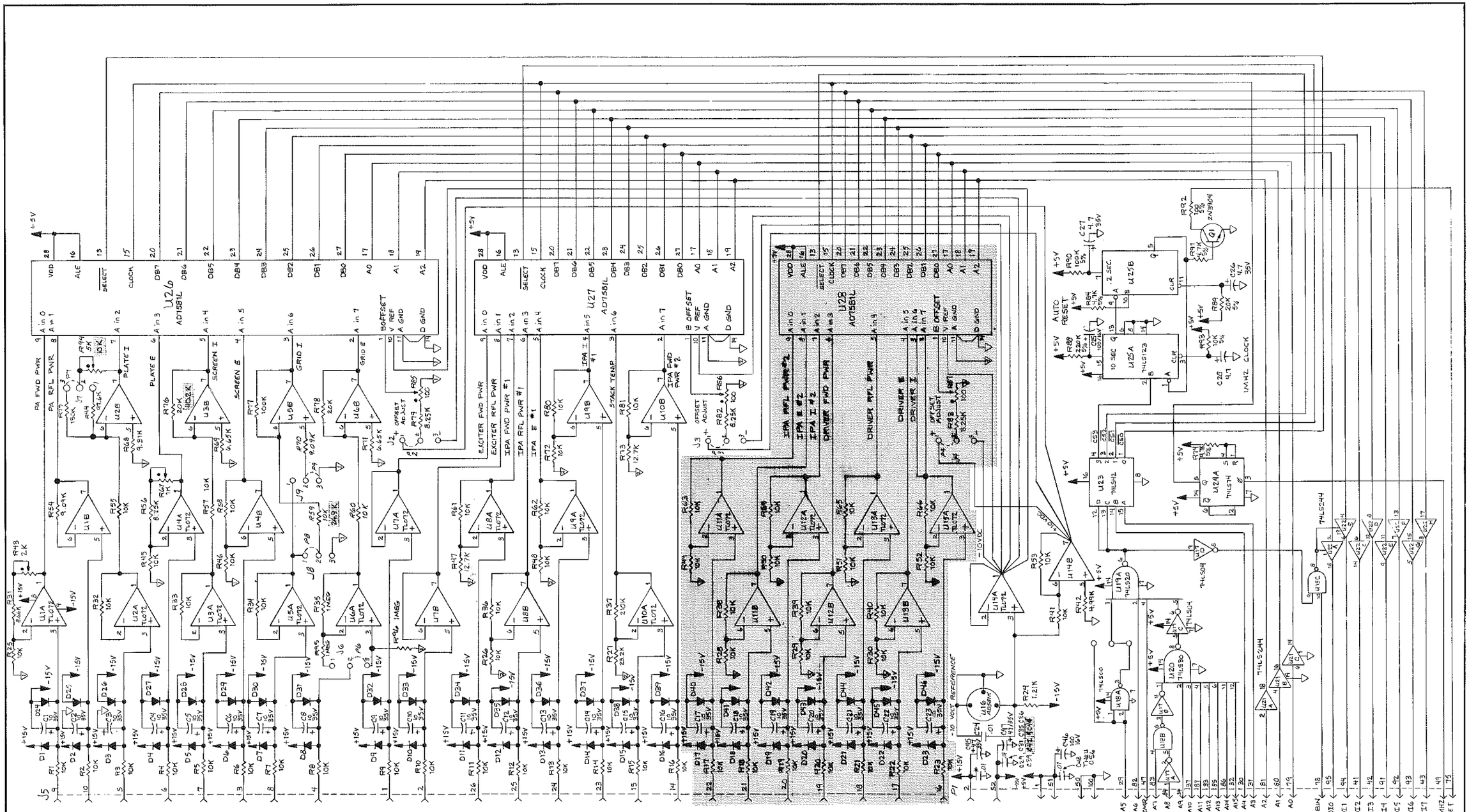
DWN. BY	MSE 4-23-84
CHKD	MH 4-24-84
ME	
PROJ. ENGR.	
MFG.	
MATERIAL	SEE B/M 918-0017
FINISH	
NEXT ASSY.	

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE PCB ASSEMBLY, 64K MEMORY BOARD

TYPE	SIZE	DWG. NO.	REV
A	C	918-0017, 919-0202	F

MODEL XMTR CONTROLLER | SCALE 2/1 | SHEET 1 OF 1



JUMPER SELECT TABLE				
	J6	J7	J8	J9
FM1.5A	1-2	1-2	2-3	1-2
FM3.5A	2-3	2-3	1-2	2-3
FM5A	2-3	2-3	1-2	2-3
FM10A	2-3	2-3	1-2	2-3
FM30A	2-3	1-2	1-2	2-3
FM35A	2-3	1-2	1-2	2-3

SEE B/M 919-0058 (FM-LOW POWER APPLICATION)
SEE B/M 919-0058-001 (FM-30 APPLICATION)

NOTES:
1. ALL RESISTORS IN OHMS, ¼W 1%; ALL DIODES 1N4005; CAPACITORS IN MICROFARADS; U.O.S.
2. * DENOTES C30, C32, C33, C34, C37, C38, C40, CH1 & CH3.
3. COMPONENTS LAST USED: C56, D46, J9, Q1, R96 & U28.
4. COMPONENTS NOT USED: U15B, U17-E&F, U18D, U19B, U21-DE, F, G&H, U24B
5. P6 TO BE IN POSITION 1-2 FOR FM-1.5 TRANSMITTER; P6 TO BE IN POSITION 2-3 FOR ALL OTHER TRANSMITTERS.
6. COMPONENTS WITHIN SHADED AREA APPLY TO FM-30 TRANSMITTER ONLY.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

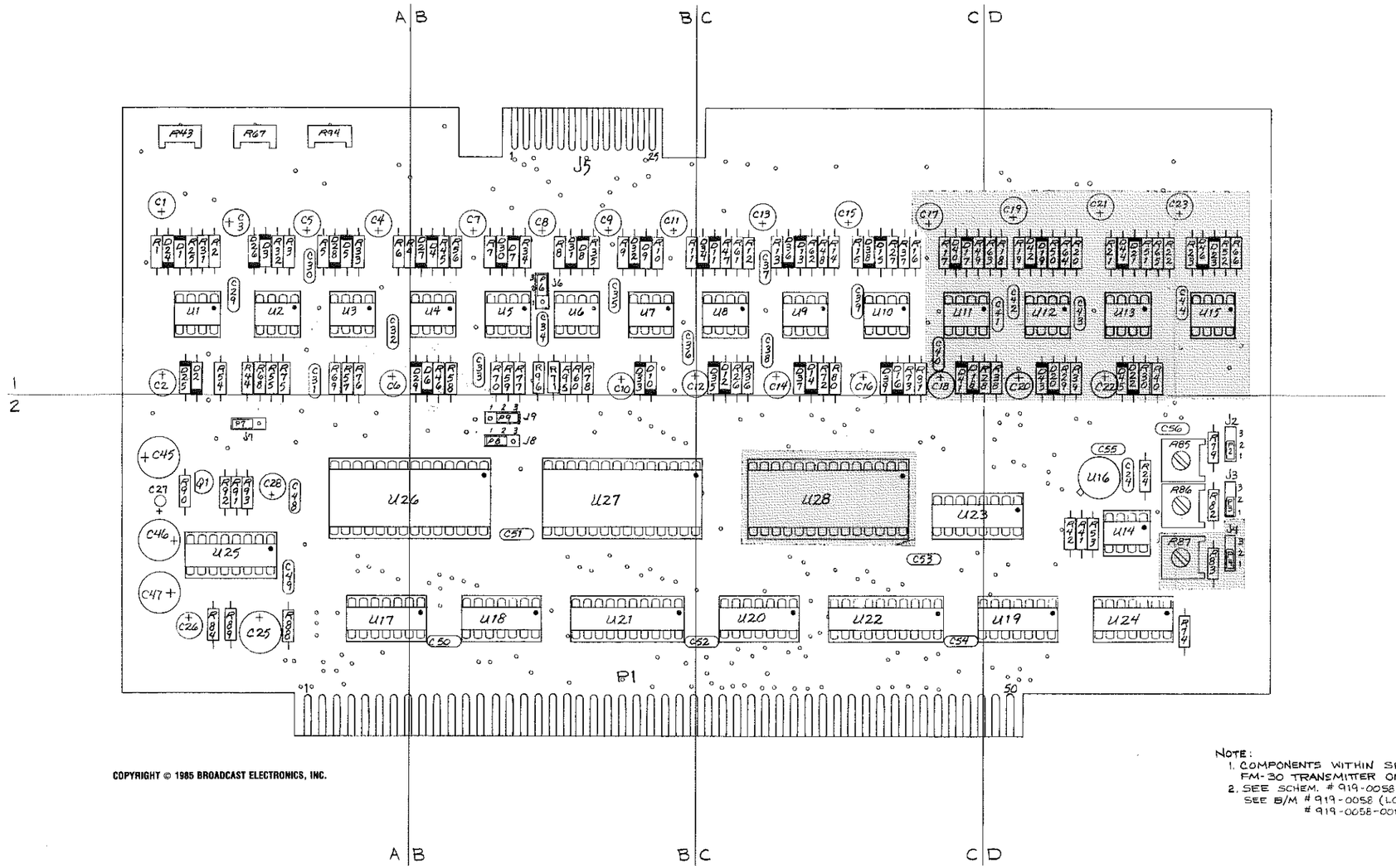
DWN. BY MJ OAF 9-12-83
CHKD J.T.H. 1-19-84
PROJ. ENGR. [signature] 1-19-84
MFG.
MATERIAL
FINISH
ME
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3505 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE SCHEMATIC
ANALOG/DIGITAL PCB

TYPE	SIZE	DWG. NO.	REV
J	D	919-0058, 919-0058-001	J

MODEL FM-XMTRS SCALE NTS SHEET 1 OF 1



NOTE:
1. COMPONENTS WITHIN SHADED AREA APPLY TO FM-30 TRANSMITTER ONLY.
2. SEE SCHEM. # 919-0058 & 919-0058-001
   SEE B/M # 919-0058 (LOW POWER XMTRS)
   # 919-0058-001 (FM-30 XMTR)

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TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY MJ DAY 9-21-83
CHKD MH 1-19-84
ME
PROJ. ENGR. 1-19-84
MFG.

MATERIAL
FINISH
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O.BOX 3506 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE PCB ASSEMBLY
ANALOG/DIGITAL PCB

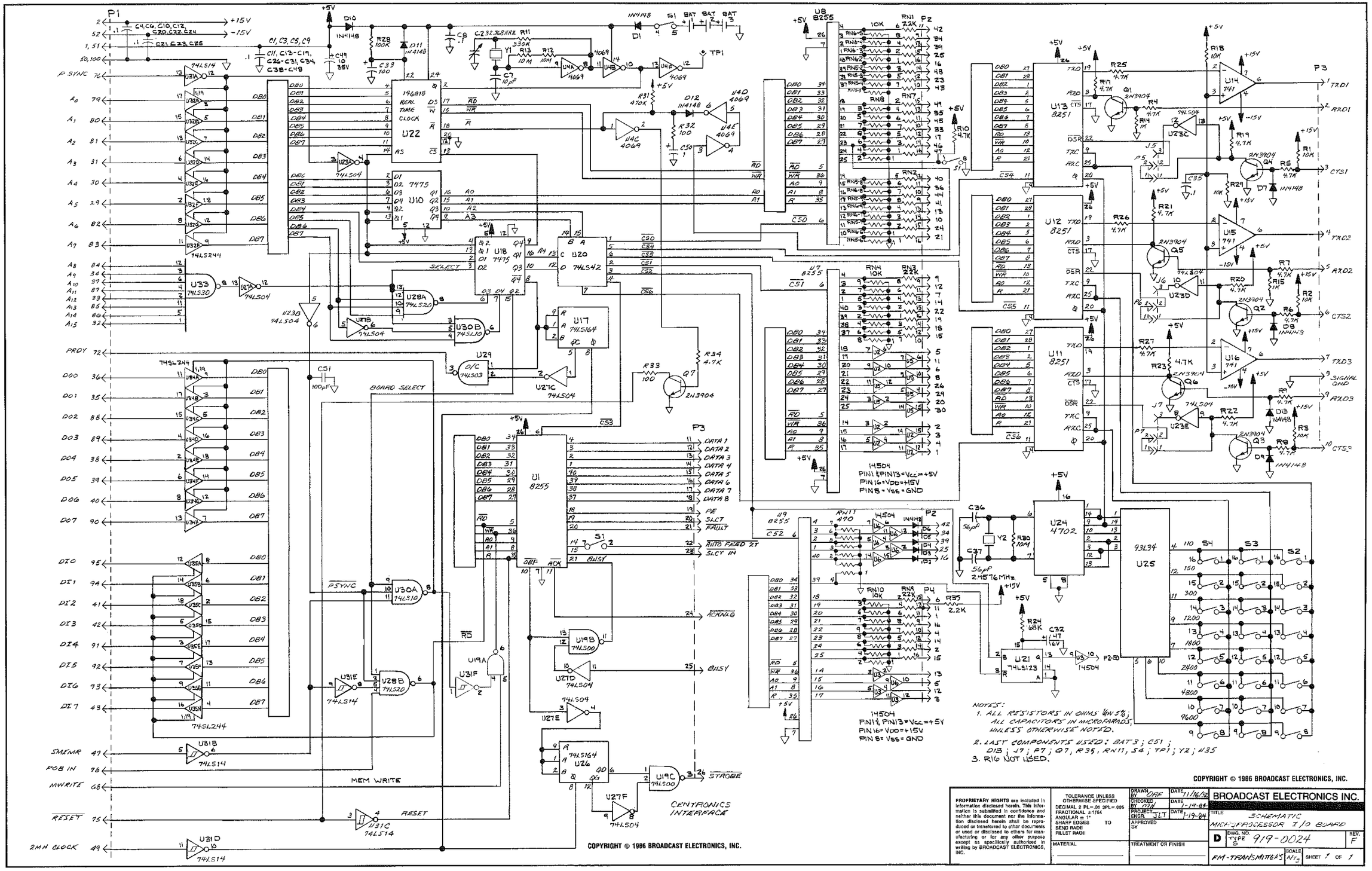
TYPE	SIZE	DWG. NO.	REV
A	D	919-0058 & 919-0058-001	J

MODEL FM-XMTRS. SCALE 2/1 SHEET 7 OF 7

REF	ZONE	REF	ZONE	REF	ZONE	REF	ZONE	REF	ZONE
C1	A1	D1	A1	P6	B1	R52	D1	U12	D1
C2	A1	D2	A1	P7	A2	R53	D2	U13	D1
C3	A1	D3	A1	P8	B2	R54	A1	U14	D2
C4	A1	D4	B1	P9	B2	R55	A1	U15	D1
C5	A1	D5	A1	Q1	A2	R56	B1	U16	D2
C6	A1	D6	B1	R1	A1	R57	A1	U17	A2
C7	B1	D7	B1	R2	A1	R58	B1	U18	B2
C8	B1	D8	B1	R3	A1	R59	B1	U19	D2
C9	B1	D9	B1	R4	A1-B1	R60	B1	U20	C2
C10	B1	D10	B1	R5	A1	R61	C1	U21	B2
C11	B1	D11	C1	R6	A1	R62	C1	U22	C2
C12	B1-C1	D12	C1	R7	B1	R63	D1	U23	C2-D2
C13	C1	D13	C1	R8	B1	R64	D1	U24	D2
C14	C1	D14	C1	R9	B1	R65	D1	U25	A2
C15	C1	D15	C1	R10	B1	R66	D1	U26	A2-B2
C16	C1	D16	C1	R11	B1	R67	A1	U27	B2
C17	C1	D17	C1	R12	C1	R68	A1	U28	C2
C18	C1	D18	C1	R13	C1	R69	A1		
C19	D1	D19	D1	R14	C1	R70	B1		
C20	D1	D20	D1	R15	C1	R71	B1		
C21	D1	D21	D1	R16	C1	R72	C1		
C22	D1	D22	D1	R17	C1	R73	C1		
C23	D1	D23	D1	R18	D1	R74	D2		
C24	D2	D24	A1	R19	D1	R75	A1		
C25	A2	D25	A1	R20	D1	R76	A1		
C26	A2	D26	A1	R21	D1	R77	B1		
C27	A2	D27	B1	R22	D1	R78	B1		
C28	A2	D28	A1	R23	D1	R79	D2		
C29	A1	D29	B1	R24	D2	R80	C1		
C30	A1	D30	B1	R25	A1	R81	C1		
C31	A1	D31	B1	R26	C1	R82	D2		
C32	A1	D32	B1	R27	C1	R83	D2		
C33	B1	D33	B1	R28	C1-D1	R84	A2		
C34	B1	D34	C1	R29	D1	R85	D2		
C35	B1	D35	C1	R30	D1	R86	D2		
C36	B1	D36	C1	R31	A1	R87	D2		
C37	C1	D37	C1	R32	A1	R88	A2		
C38	C1	D38	C1	R33	A1	R89	A2		
C39	C1	D39	C1	R34	B1	R90	A2		
C40	C1	D40	C1	R35	B1	R91	A2		
C41	D1	D41	C1	R36	C1	R92	A2		
C42	D1	D42	D1	R37	C1	R93	A2		
C43	D1	D43	D1	R38	D1	R94	A1		
C44	D1	D44	D1	R39	D1	R95	B1		
C45	A2	D45	D1	R40	D1	R96	B1		
C46	A2	D46	D1	R41	D2	U1	A1		
C47	A2	J2	D2	R42	D2	U2	A1		
C48	A2	J3	D2	R43	A1	U3	A1		
C49	A2	J4	D2	R44	A1	U4	B1		
C50	B2	J6	B1	R45	B1	U5	B1		
C51	B2	J7	A2	R46	B1	U6	B1		
C52	B2	J8	B2	R47	C1	U7	B1		
C53	C2	J9	B2	R48	C1	U8	C1		
C54	C2	P2	D2	R49	C1	U9	C1		
C55	D2	P3	D2	R50	D1	U10	C1		
C56	D2	P4	D2	R51	D1	U11	C1		

597-0036-21

FIGURE 7-5. COMPONENT LOCATOR, ANALOG/DIGITAL CIRCUIT BOARD



TOLERANCE UNLESS OTHERWISE SPECIFIED
DECIMAL 2 PL = .01 3PL = .005
FRACTIONAL ±1/64
ANGULAR = 1°
SHARP EDGES TO BEND RADII
FILLET RADII

MATERIAL

TREATMENT OR FINISH

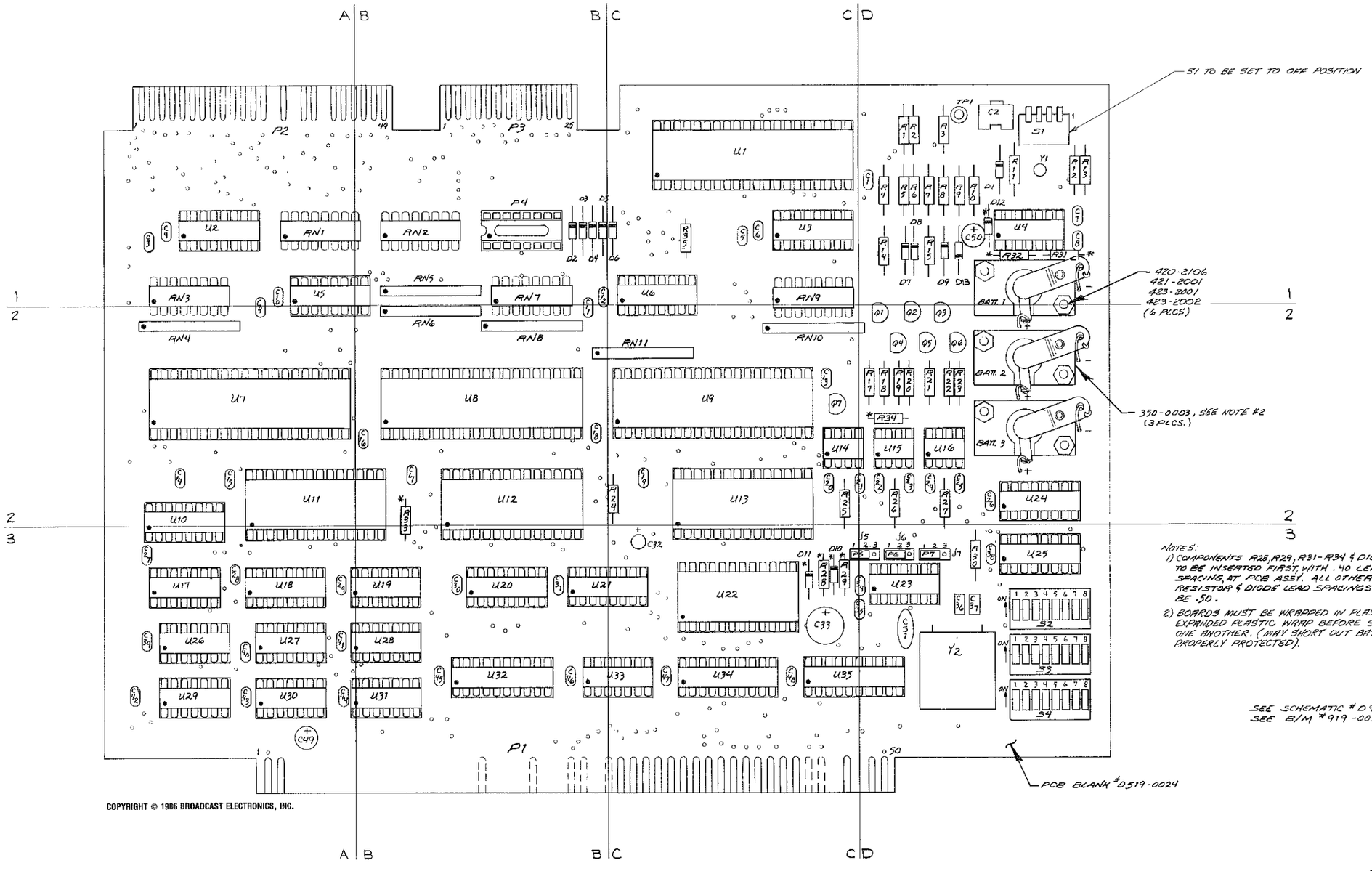
DRAWN ORF DATE 11/16/82
CHECKED DATE 1-19-84
PROJECT ENGR. JLT DATE 1-19-84
APPROVED BY

BROADCAST ELECTRONICS INC.

TITLE SCHEMATIC MICROPROCESSOR I/O BOARD

D DWG. NO. TYPE S 919-0024 REV. F

FM-TRANSMITTERS SCALE NTS SHEET 1 OF 1



NOTES:

1) COMPONENTS R28, R29, R31-R34 & D10-D12 TO BE INSERTED FIRST, WITH .40 LEAD SPACING, AT PCB ASSY. ALL OTHER RESISTOR & DIODE LEAD SPACINGS TO BE .50.

2) BOARDS MUST BE WRAPPED IN PLASTIC, BUBBLE PACK, OR EXPANDED PLASTIC WRAP BEFORE STACKING ON TOP OF ONE ANOTHER. (MAY SHORT OUT BATTERIES IF NOT PROPERLY PROTECTED).

SEE SCHEMATIC #0919-0024
SEE B/M #919-0024

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TOLERANCE UNLESS OTHERWISE SPECIFIED
DECIMAL 2 PL=.01 3PL=.005
FRACTIONAL ±1/64
ANGULAR ±1°
SHARP EDGES TO BEND RADII
FILLET RADII

MATERIAL

DRAWN BY ORF DATE 6-6-83
CHECKED BY MM DATE 7-19-84
PROJECT ENGR. MM DATE 7-19-84
APPROVED BY

TREATMENT OR FINISH

BROADCAST ELECTRONICS INC.

TITLE PCB ASSEMBLY MICROPROCESSOR I/O BOARD

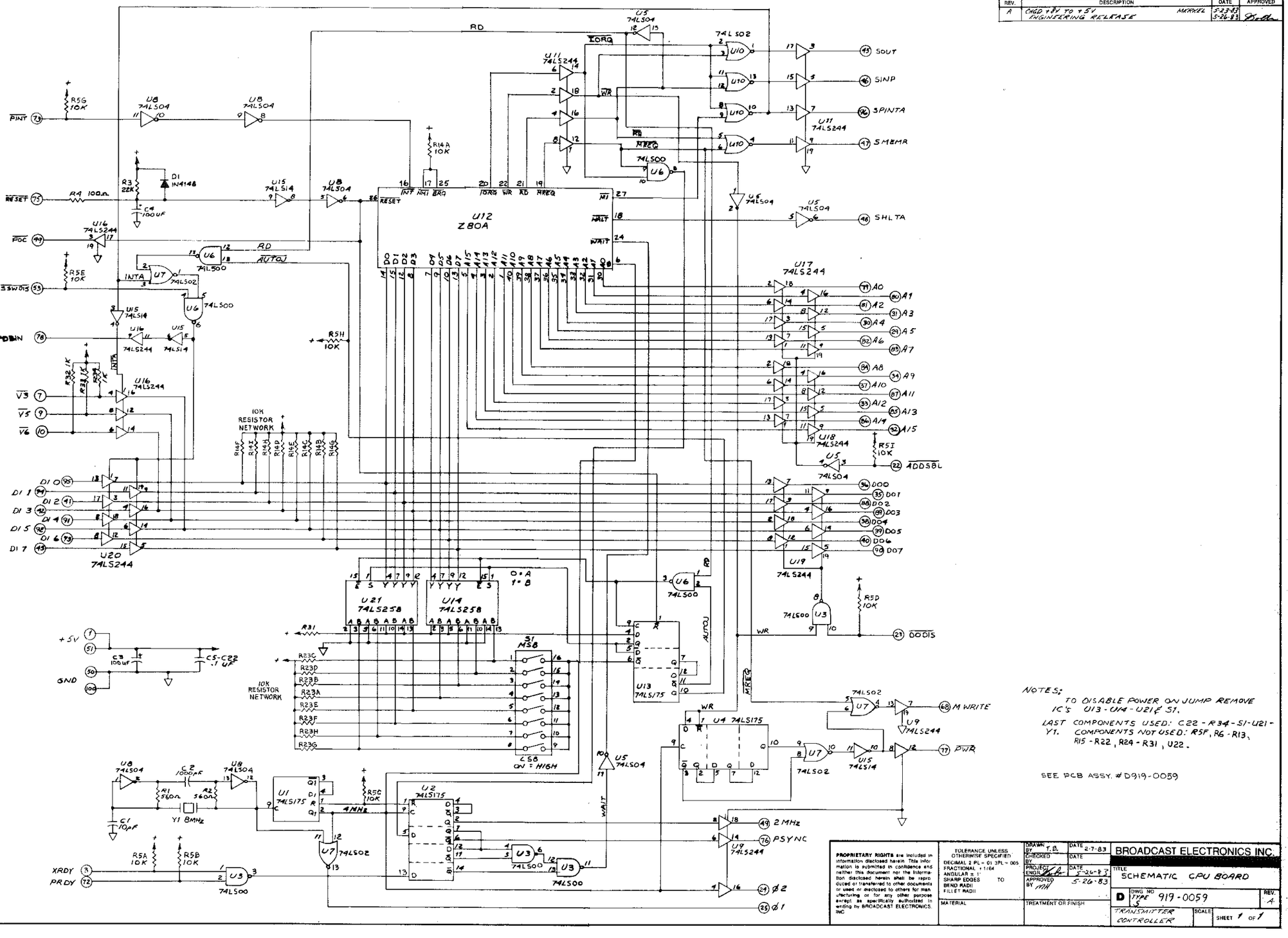
D DWG. NO. TYPE A 919-0024 REV. H

FM TRANSMITTER SCALE 2/1 SHEET 1 OF 1

REF	ZONE	REF	ZONE	REF	ZONE	REF	ZONE
BAT1	D1	D1	D1	R28	C3	U31	B3
BAT2	D2	D2	B1	R29	C3	U32	B3
BAT3	D2	D3	B1	R30	D3	U33	B3-C3
C1	D1	D4	B1	R31	D1	U34	C3
C2	D1	D5	B1	R32	D1	U35	C3-D3
C3	A1	D6	C1	R33	B2	Y1	D1
C4	A1	D7	D1	R34	D2	Y2	D3
C5	C1	D8	D1	R35	C1		
C6	C1	D9	D1	RN1	A1		
C7	D1	D10	C3	RN2	B1		
C8	D1	D11	C3	RN3	A1		
C9	A1-A2	D12	D1	RN4	A2		
C10	A1	J5	C3-D3	RN5	B1		
C11	B1-B2	J6	D3	RN6	B2		
C12	B1	J7	D3	RN7	B1		
C13	C2	P4	B1	RN8	B2		
C14	A2	P5	C3-D3	RN9	C1		
C15	A2	P6	D3	RN10	C1		
C16	B2	P7	D3	RN11	C1		
C17	B2	Q1	D2	S1	D1		
C18	B2	Q2	D2	S2	D3		
C19	C2	Q3	D2	S3	D3		
C20	C2	Q4	D2	S4	D3		
C21	C2-D2	Q5	D2	U1	C1		
C22	D2	Q6	D2	U2	A1		
C23	D2	Q7	C2	U3	C1		
C24	D2	R1	D1	U4	D1		
C25	D2	R2	D1	U5	A1		
C26	D2	R3	D1	U6	C1		
C27	A3	R4	D1	U7	A2		
C28	A3	R5	D1	U8	B2		
C29	A3	R6	D1	U9	C2		
C30	B3	R7	D1	U10	A2-A3		
C31	B3	R8	D1	U11	A2		
C32	C3	R9	D1	U12	B2		
C33	C3	R10	D1	U13	C2		
C34	C3-D3	R11	D1	U14	C2		
C35	C3-D3	R12	D1	U15	D2		
C36	D3	R13	D1	U16	D2		
C37	D3	R14	D1	U17	A3		
C38	D3	R15	D1	U18	A3		
C39	A3	R16	D1	U19	B3		
C40	A3	R17	D2	U20	B3		
C41	A3	R18	D2	U21	B3-C3		
C42	A3	R19	D2	U22	C3		
C43	A3	R20	D2	U23	D3		
C44	A3	R21	D2	U24	D2		
C45	B3	R22	D2	U25	D3		
C46	B3	R23	D2	U26	A3		
C47	C3	R24	C2	U27	A3		
C48	C3	R25	C2	U28	B3		
C49	A3	R26	D2	U29	A3		
C50	D1	R27	D2	U30	A3		

FIGURE 7-8. COMPONENT LOCATOR, INPUT/OUTPUT CIRCUIT BOARD

REVISIONS				
REV.	DESCRIPTION		DATE	APPROVED
A	CHGD +8V TO +5V ENGINEERING RELEASE	MARKEL	5-23-83 5-26-83	



NOTES:

TO DISABLE POWER ON JUMP REMOVE IC'S U13 - U14 - U21 & S1.

LAST COMPONENTS USED: C22 - R34 - S1 - U21 - Y1. COMPONENTS NOT USED: R5F, R6 - R13, R15 - R22, R24 - R31, U22.

SEE PCB ASSY. # D919-0059

TOLERANCE UNLESS OTHERWISE SPECIFIED
DECIMAL 2 PL = 01 3PL = 005
FRACTIONAL ± 1/64
ANGULAR ± 1°
SHARP EDGES TO BEND RADII
FILLET RADII
MATERIAL
TREATMENT OR FINISH

DRAWN BY T.B. DATE 2-7-83
CHECKED BY DATE
PROJECT ENGR. DATE 5-26-83
APPROVED BY 5-26-83

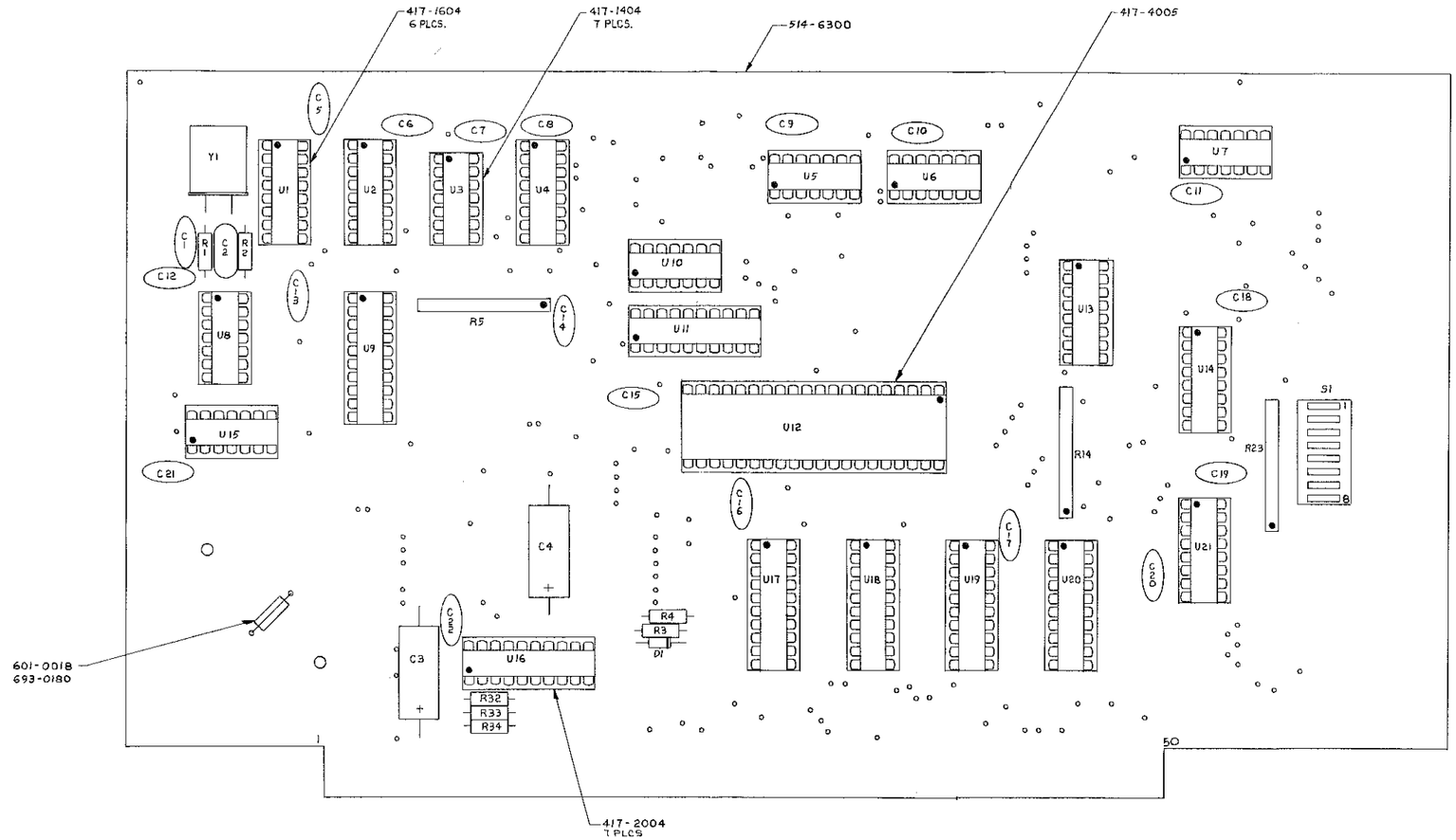
BROADCAST ELECTRONICS INC.

TITLE SCHEMATIC CPU BOARD

D DWG NO TYPE S 919-0059 REV. A

TRANSMITTER CONTROLLER SCALE SHEET 1 OF 1

REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
A	SHOWED POLARITY ON U16 MERKEL ENGINEERING RELEASE	5-23-83 5-26-83	[illegible]
B	LABELED S1-1 AND S1-8.	6-9-84	MH



SEE B/M # 919-0059
SEE SCHEMATIC # D919-0059

TOLERANCE UNLESS OTHERWISE SPECIFIED
DECIMAL 2 PL=.01 3PL=.005
FRACTIONAL ±1/64
ANGULAR ± 1°
SHARP EDGES TO
BEND RADII
FILLET RADII

MATERIAL

DRAWN BY T.B. DATE 2-4-83
CHECKED BY DATE
PROJECT ENGR. DATE 5-26-83
APPROVED BY MH 5-26-83

TREATMENT OR FINISH

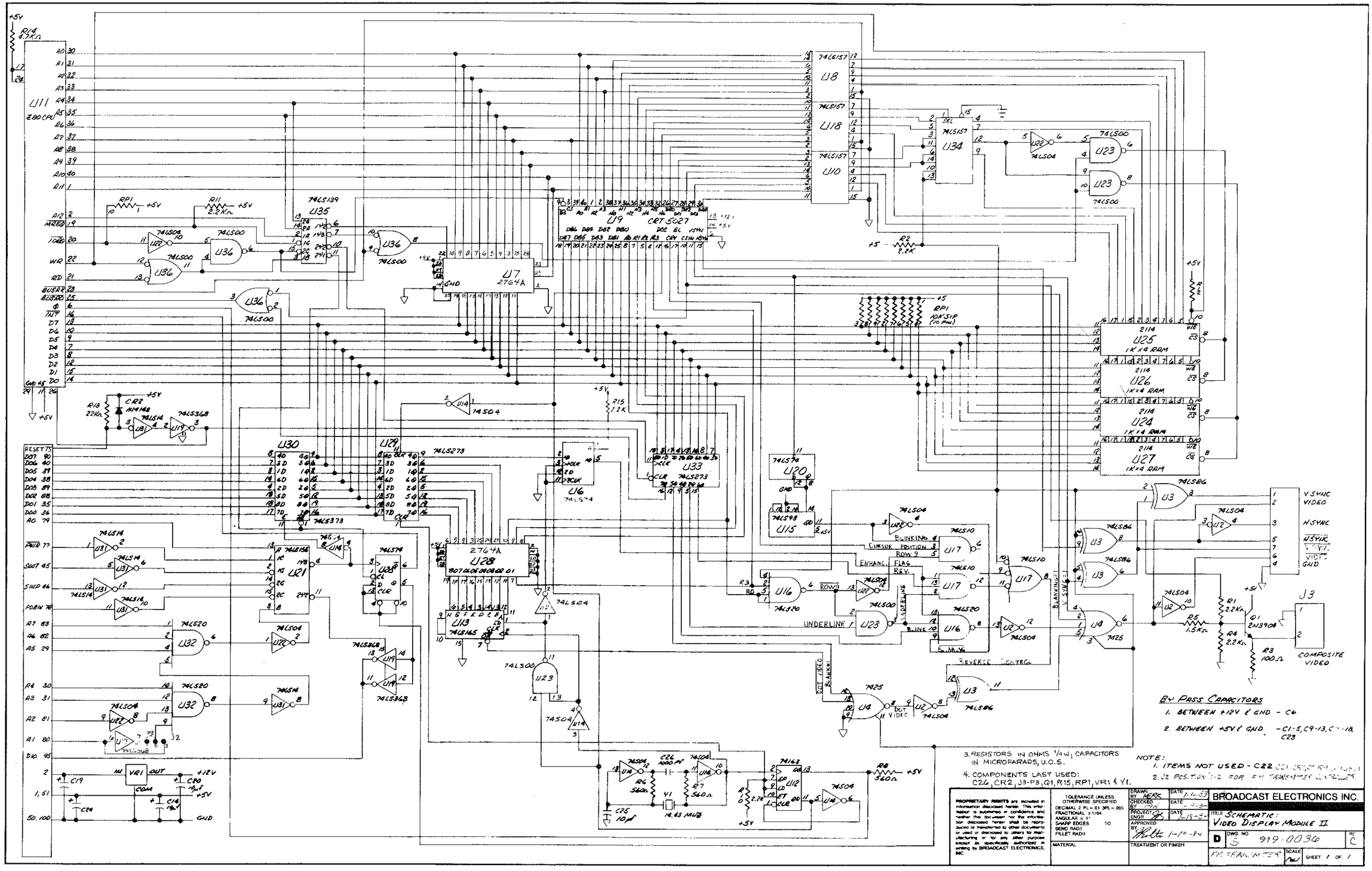
BROADCAST ELECTRONICS INC.

TITLE PCB ASSEMBLY CPU BOARD

D DWG. NO. TYPE A 919-0059 REV. B

TRANSMITTER CONTROLLER

SCALE 2/1 SHEET 1 OF 1


U11 Z80 CPU
U8 74LS157
U18 74LS157
U10 74LS157
U19 CRT 5027
U7 2764A
U35 74LS139
U36 74LS00
U34 74LS157
U22 74LS08
U23 74LS00
U25 2114 1K x 4 RAM
U26 2114 1K x 4 RAM
U24 2114 1K x 4 RAM
U27 2114 1K x 4 RAM
U30 74LS373
U29 74LS273
U33 74LS273
U6 74LS74
U20 74LS74
U15 74LS08
U21 74LS138
U28 2764A
U13 74LS165
U14 74LS04
U31 74LS14
U32 74LS20
U19 74LS368
U16 74LS20
U17 74LS10
U23 74LS00
U12 74LS04
U3 74LS86
U4 7425
U2 74LS04
U12 74S04
VR1
RP1 10K SIP (10 PIN)
J3 COMPOSITE VIDEO
Q1 2N3904
R1 2.2KΩ
R4 2.2KΩ
R5 1.5KΩ
R3 100Ω
R8 560Ω
R7 560Ω
R6 560Ω
C25 10pf
14.43 MHz
C26 1000 pf
C19 10µf
C20 10µf
C21 10µf
C24
RESET 75
V SYNC
H SYNC
VIDEO GND
BLANKING
CURSOR POSITION ROW 9
ENHANC. FLAG REV.
UNDERLINE
BLINK
REVERSE CONTRL
DOT VIDEO
BLANKING
BY PASS CAPACITORS
1. BETWEEN +12V & GND - C6
2. BETWEEN +5V & GND - C1-5, C9-13, C15-18, C23
3. RESISTORS IN OHMS 1/4W; CAPACITORS IN MICROFARADS, U.O.S.
4. COMPONENTS LAST USED: C26, CR2, J3-P3, Q1, R15, RP1, VR1 & Y1.
NOTE:
1. ITEMS NOT USED - C22
2. J2 POS. 1 & 2 FOR FM TRANSMITTER OUTPUTS.
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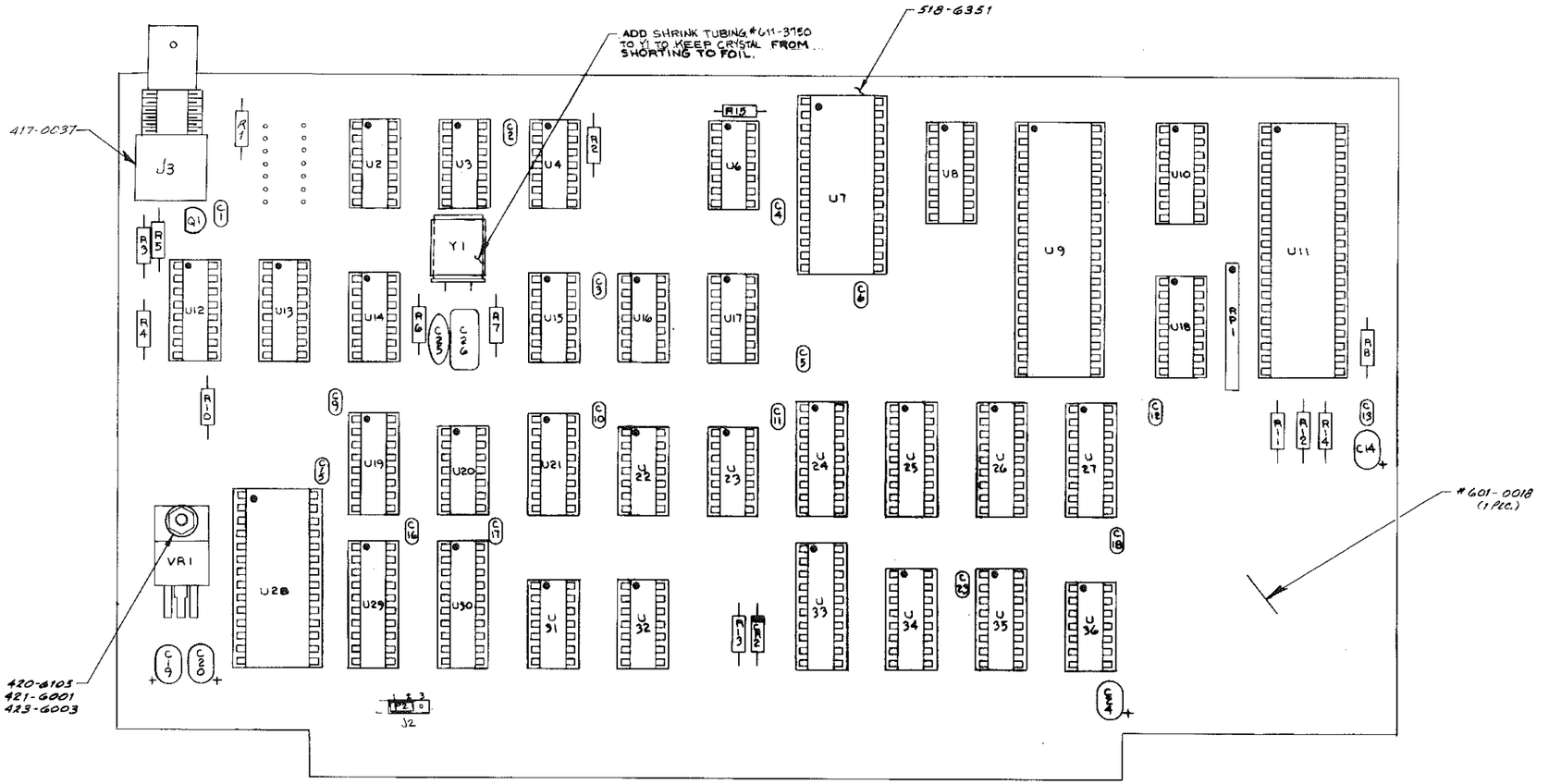
TOLERANCE UNLESS OTHERWISE SPECIFIED
DECIMAL 2 PL = .01 3PL = .005
FRACTIONAL ±1/64
ANGULAR ± 1°
SHARP EDGES TO
BEND RADII
FILLET RADII
MATERIAL
TREATMENT OR FINISH
DRAWN BY MERK DATE 1-14-83
CHECKED BY DATE
PROJECT ENGR DATE 1-15-84
APPROVED BY DATE 1-14-84
BROADCAST ELECTRONICS INC.
TITLE SCHEMATIC: VIDEO DISPLAY MODULE II
D DWG. NO S 919-0036 REV C
FM TRANSMITTER
SCALE NONE
SHEET 1 OF 1



SEE B/M # 919-0036
SEE SCHEMATIC D 919-0036

TOLERANCE UNLESS OTHERWISE SPECIFIED
DECIMAL 2 PL = .01 3PL = .005
FRACTIONAL ± 1/64
ANGULAR ± 1°
SHARP EDGES TO
BEND RADII
FILLET RADII
MATERIAL
TREATMENT OR FINISH

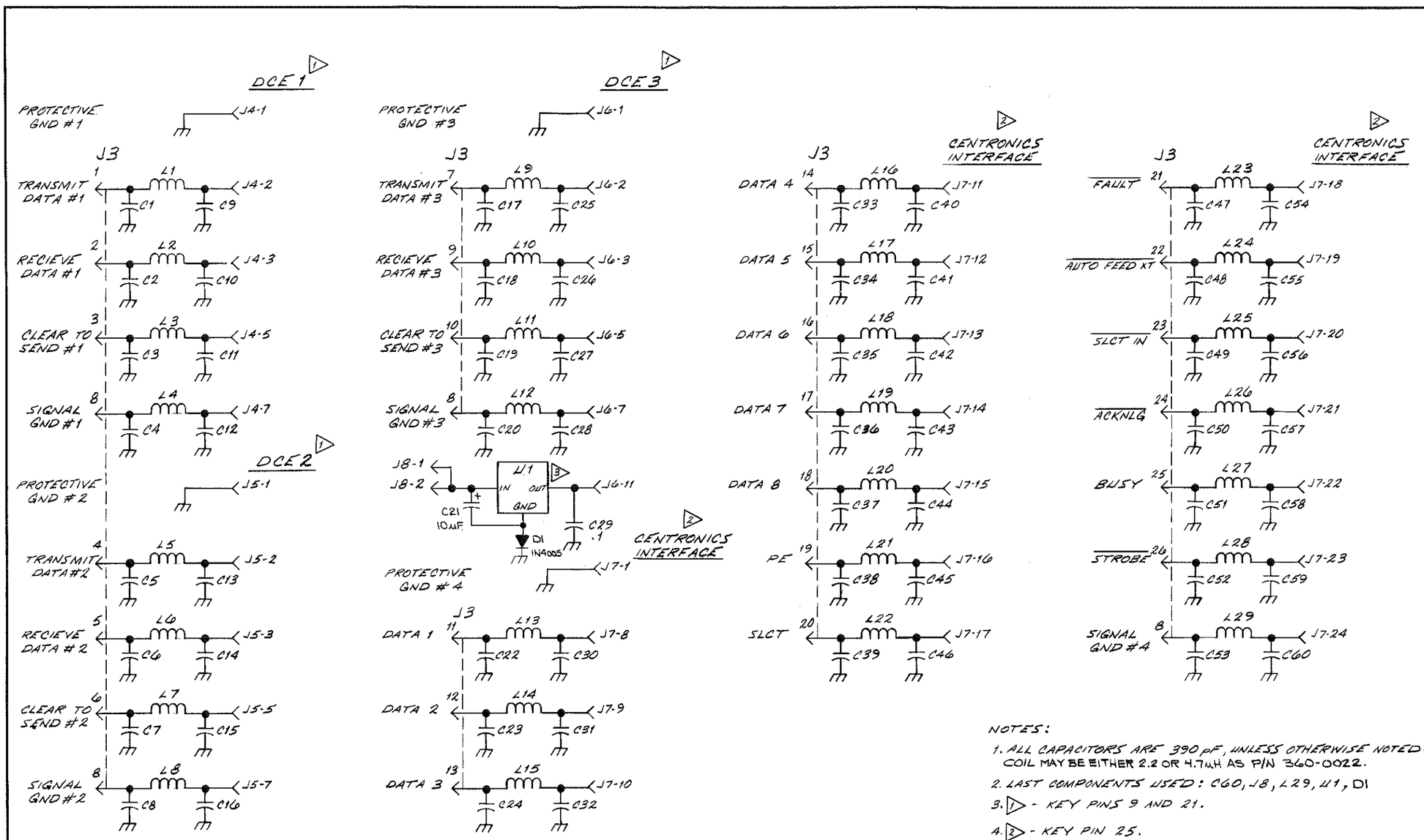
DRAWN BY MARKEL DATE 1-19-89
CHECKED BY [illegible] DATE 1-19-89
PROJECT ENGR. [illegible] DATE 1-18-89
APPROVED BY [illegible] 1-18-89

BROADCAST ELECTRONICS INC.

TITLE P.C.B ASSEMBLY VIDEO DISPLAY MODULE II

D | DWG. NO. TYPE A | 919-0036 | REV. C

FM TRANSMITTER | SCALE 2/1 | SHEET 1 OF 1



NOTES:

1. ALL CAPACITORS ARE 390 pF, UNLESS OTHERWISE NOTED. COIL MAY BE EITHER 2.2 OR 4.7 uH AS P/N 360-0022.
2. LAST COMPONENTS USED: C60, J8, L29, U1, D1
3. [1] - KEY PINS 9 AND 21.
4. [2] - KEY PIN 25.
5. [3] - HEATSINK REQUIRED, BE P/N 455-7805
6. PINS J6-25, J5-24, J4-23 & J7-4 ARE USED FOR KEYING PINS

SEE ASSEMBLY #C919-0057
SEE B/M #919-0057

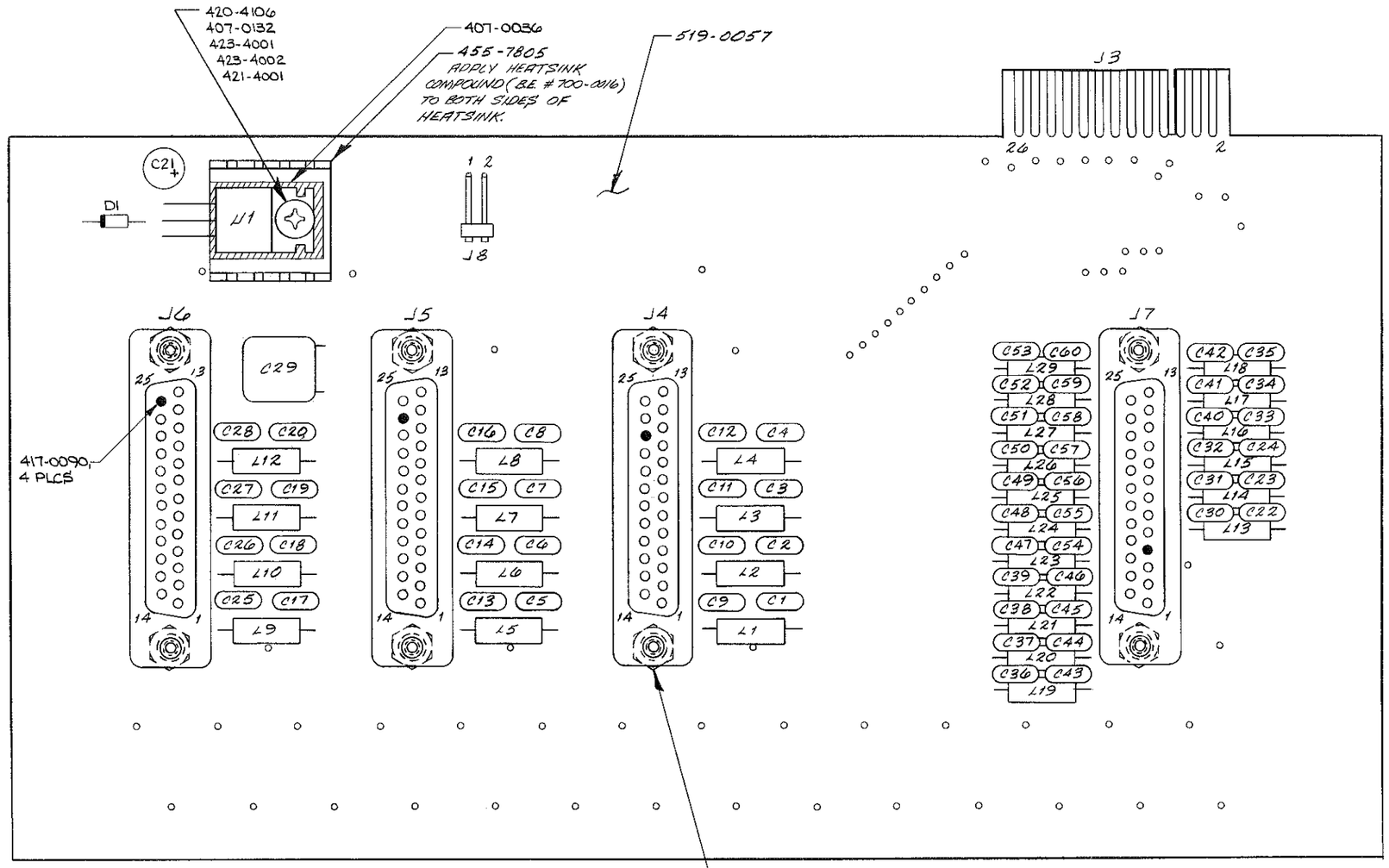
TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .XXX ± .005
.XX ± .015 ANGLES ± 1°

DWN. BY	MERKEL 1-27-83
CHKD.	
ME	
EE	1-19-84
PROJ. ENGR.	1-19-84
DFTG. SUPVR.	1-19-84
MFG.	

NEXT ASSY 959-0046
PRODUCT USED ON FM-XMTRS
FINISH —

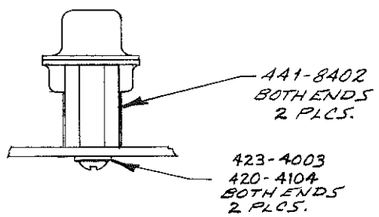
BROADCAST ELECTRONICS INC.
4100 N. 24TH ST. QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BCST ELECT QUI

TITLE PCB SCHEMATIC — MICROPROCESSOR EMI FILTER BOARD
SHEET 1 OF 1
SCALE —
REV D
TYPE 5
SIZE C
DWG. NO. 919-0057



NOTE:
L1 - L28 MAY BE EITHER 2.2 OR 4.7 μH AS P/N 360-0022

DETAIL "A"



TOLERANCE (DECIMAL) U.O.S.
.X ± .030 .XXX ± .005
.XX ± .015 ANGLES ± 1°

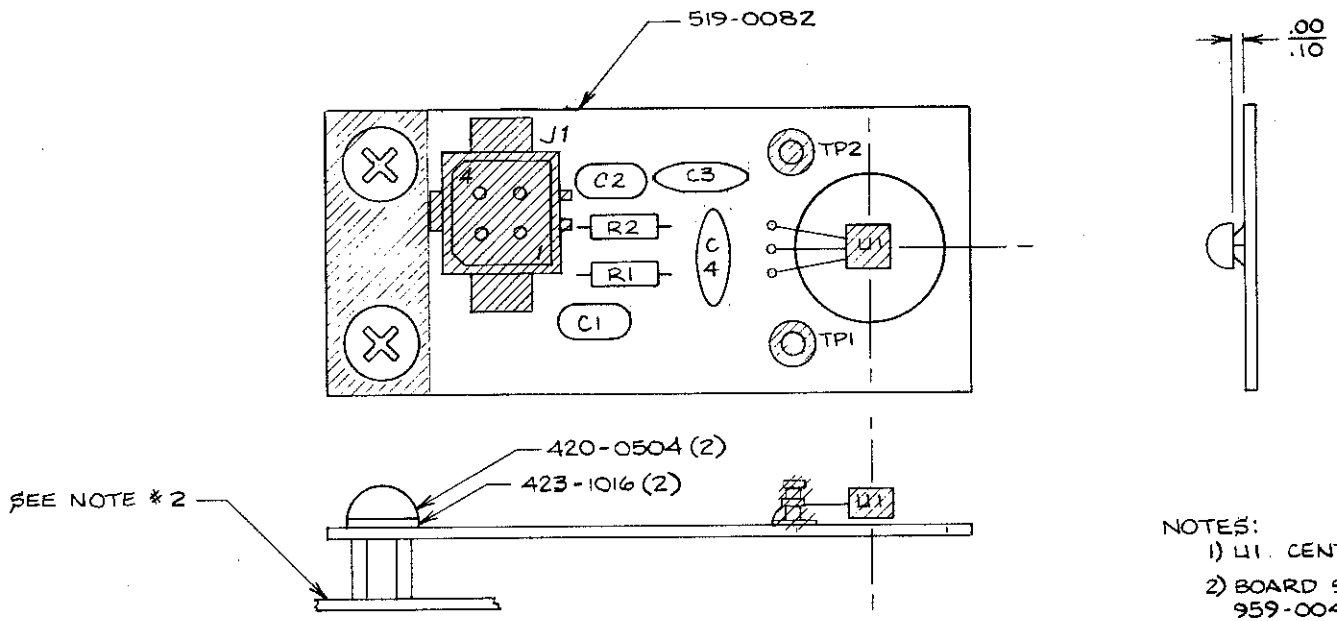
DWN. BY	MERKEL 1-26-83
CHKD.	
ME	
EE	1-19-84
PROJ. ENGR.	1-19-84
DEPT. SUPVR.	MH 1-19-84
MFG.	

NEXT ASSY. 959-0046
PRODUCT USED ON FM-XMTRS
FINISH

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST. QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BCST ELECT QUI

TITLE PCB ASSEMBLY — MICROPROCESSOR EMI FILTER BOARD

SHEET 1 OF 1
SCALE 2/1
REV E
TYPE A
SIZE C
DWG. NO. 919-0057



NOTES:
1) U1 CENTERED IN .630 HOLE.
2) BOARD SHOWN MOUNTED TO 959-0048 SHIELD CELL ASM.
3) SEE SCHEMATIC 919-0082
4) COVER WITH URETHANE CONFORMAL COATING (700-0126) AFTER COMPONENTS ARE SOLDERED. SEE COATING INSTRUCTIONS.

COATING INSTRUCTIONS:
1) MASK BODY OF DEVICE U1 COMPLETELY, MASK TURRETS TP1 + TP2, INSERT 418-0240 DUMMY PLUG IN J1, AND MASK BOTH SIDES OF PCB AT MOUNTING HOLE END AS SHADED.
2) APPLY ONE COAT OF 700-0126, SPRAY ON BOTH SIDES, PER VENDOR INSTRUCTIONS, THEN REMOVE MASKING.
3) ALLOW 15 MINS. DRYING TIME.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

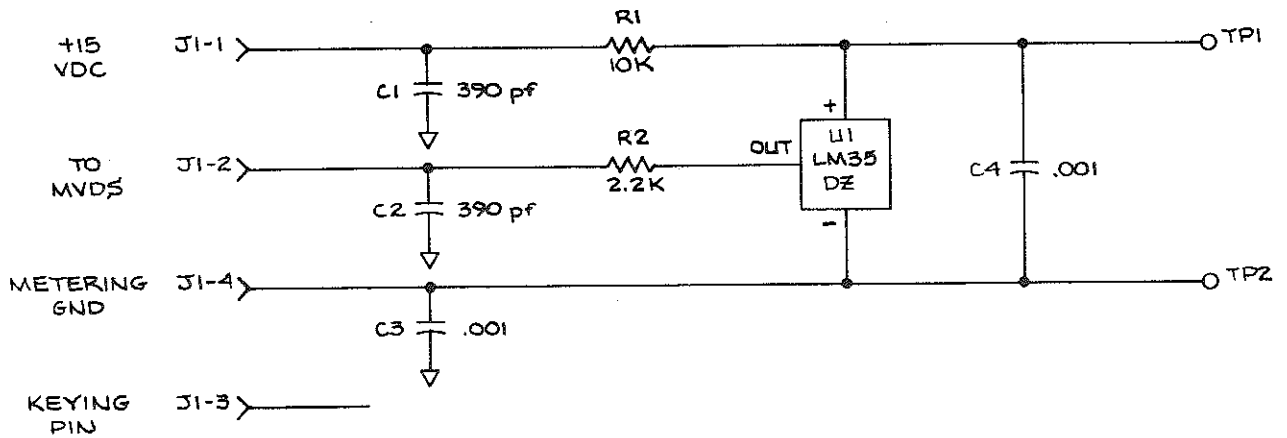
DWN. BY MSE 5-17-84
CHKD MH 5-22-84
ME
PROJ. ENGR. JMK 5-31-84
MFG.

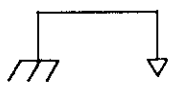
MATERIAL SEE B/M 919-0082
FINISH
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O.BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE ASM., PCB EXHAUST AIR TEMPERATURE SENSOR
TYPE A | SIZE B | DWG. NO. 919-0082 | REV B
MODEL FM3.5A/5A MVDS OPTION | SCALE 2/1 | SHEET 1 OF 1

REVISIONS					
REV	DATE	DESCRIPTION	DFTSMN	ENGR	ECN
A	5-22-84	ENGINEERING RELEASE	MB	[illegible]	—





NOTES:
1) ALL RESISTORS IN OHMS 1/4 WATT, 5%, ALL CAPACITORS IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
2) LAST COMPONENT USED: C4, J1, R2, TP2, U1

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

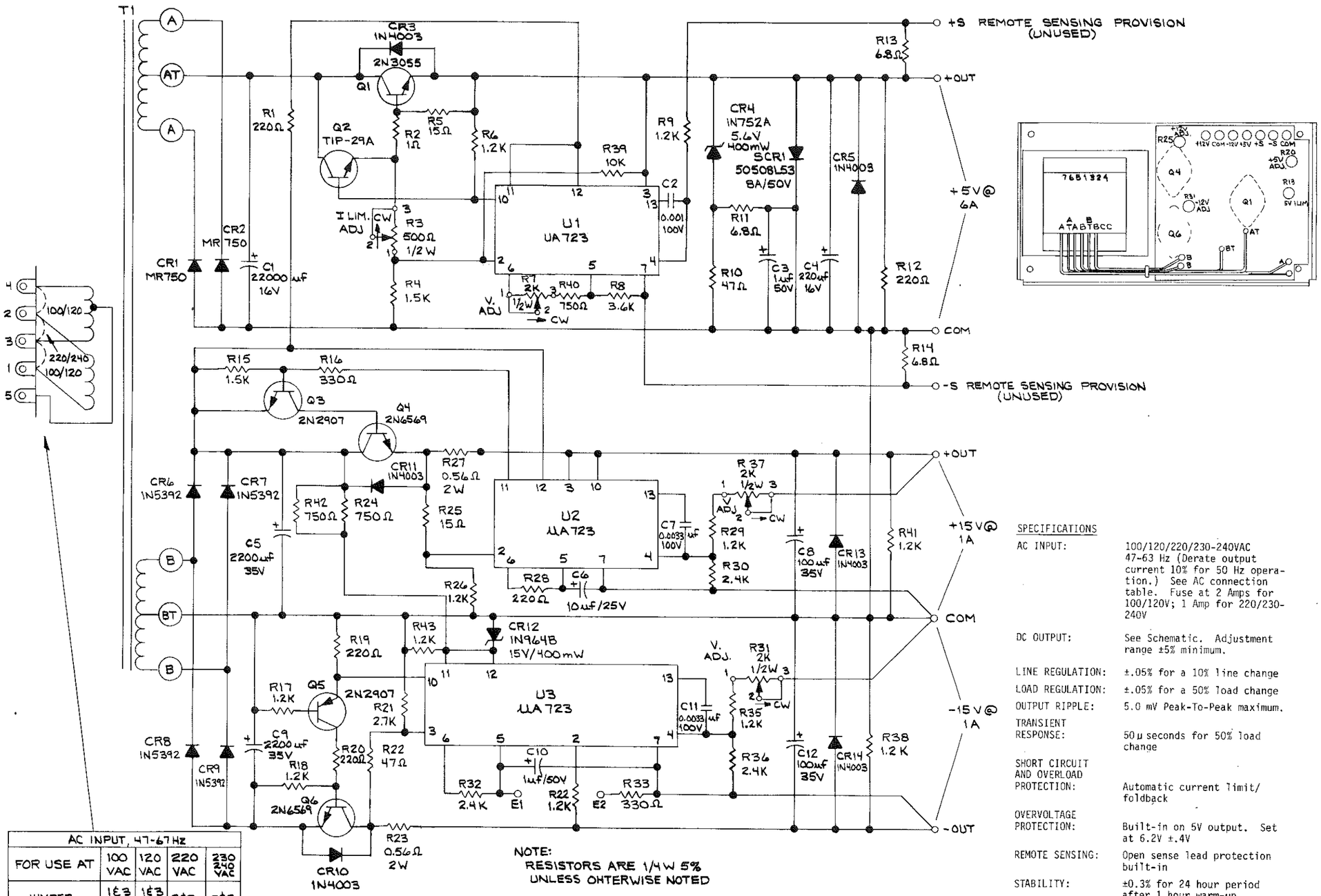
DWN. BY MSE 5-17-84
CHKD MA 5-22-84
ME
PROJ. ENGR. JTM 5-22-84
MFG
MATERIAL
FINISH
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O.BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE SCHEMATIC, EXHAUST AIR TEMPERATURE SENSOR, PCB

TYPE	SIZE	DWG. NO.	REV
S	B	919-0082	A

MODEL FM3.5A/5A MVDS OPTION | SCALE ~ | SHEET 1 OF 1



AC INPUT, 47-67 Hz				
FOR USE AT	100 VAC	120 VAC	220 VAC	230 240 VAC
JUMPER	1&3 2&4	1&3 2&4	2&3	2&3
APPLY AC	1&5	4&1	1&4	4&1

TOLERANCE FOR 100/120/220 VAC OPERATION IS +10%, -13%
TOLERANCE FOR 230/240 VAC OPERATION IS +15%, -10%

NOTE:
RESISTORS ARE 1/4W 5%
UNLESS ONTERWISE NOTED

SPECIFICATIONS

AC INPUT:	100/120/220/230-240VAC 47-63 Hz (Derate output current 10% for 50 Hz operation.) See AC connection table. Fuse at 2 Amps for 100/120V; 1 Amp for 220/230-240V
DC OUTPUT:	See Schematic. Adjustment range ±5% minimum.
LINE REGULATION:	±.05% for a 10% line change
LOAD REGULATION:	±.05% for a 50% load change
OUTPUT RIPPLE:	5.0 mV Peak-To-Peak maximum.
TRANSIENT RESPONSE:	50 μ seconds for 50% load change
SHORT CIRCUIT AND OVERLOAD PROTECTION:	Automatic current limit/ foldback
OVERVOLTAGE PROTECTION:	Built-in on 5V output. Set at 6.2V ±.4V
REMOTE SENSING:	Open sense lead protection built-in
STABILITY:	±0.3% for 24 hour period after 1 hour warm-up
TEMPERATURE RATING:	0°C to 50°C full-rated, derated linearly to 40% at 70°C
TEMPERATURE COEFFICIENT:	±.03%/°C maximum
EFFICIENCY: (Typical)	5V 45%; 15V 55%

597-0036-23

FIGURE 7-17. SCHEMATIC DIAGRAM POWER SUPPLY

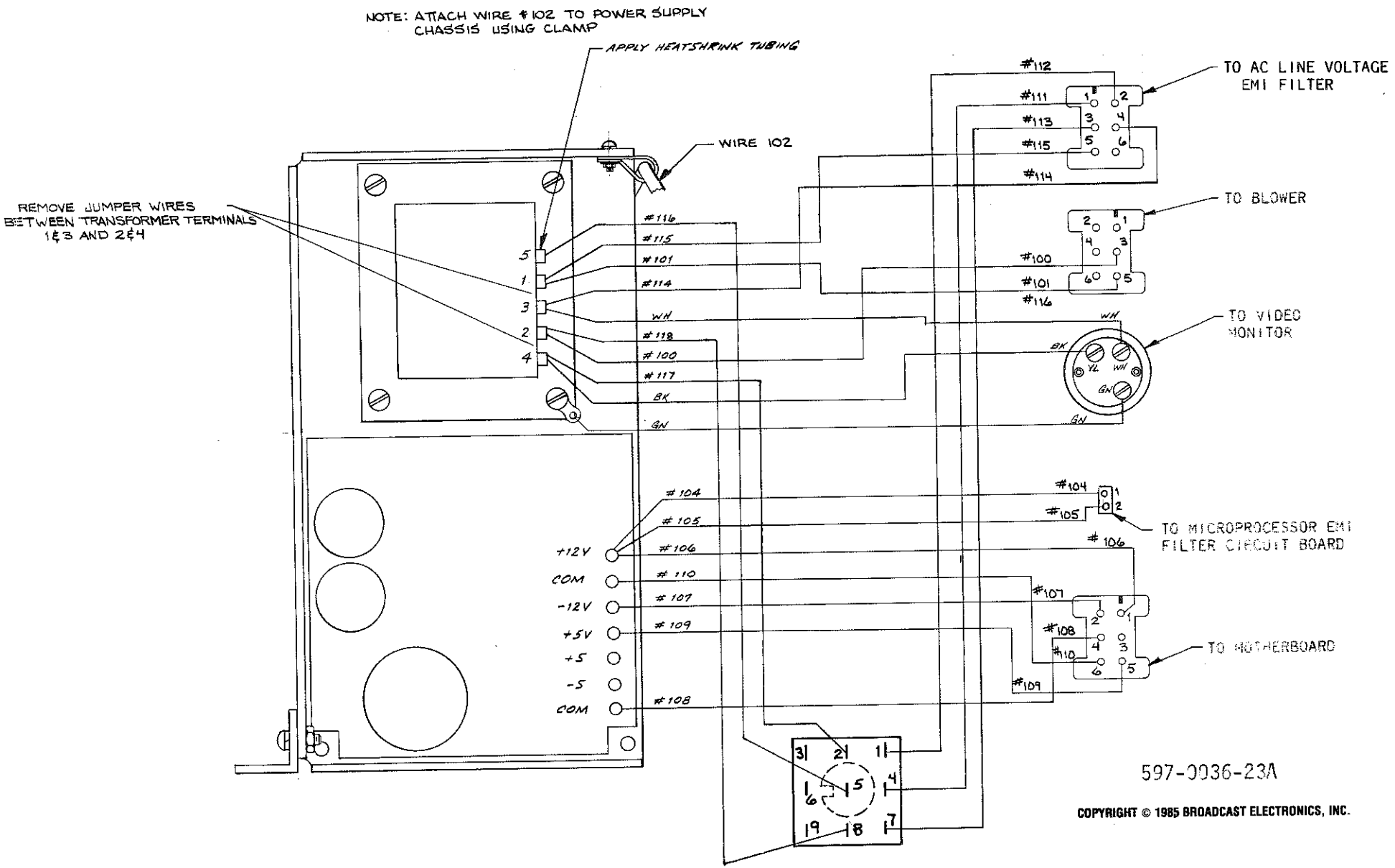
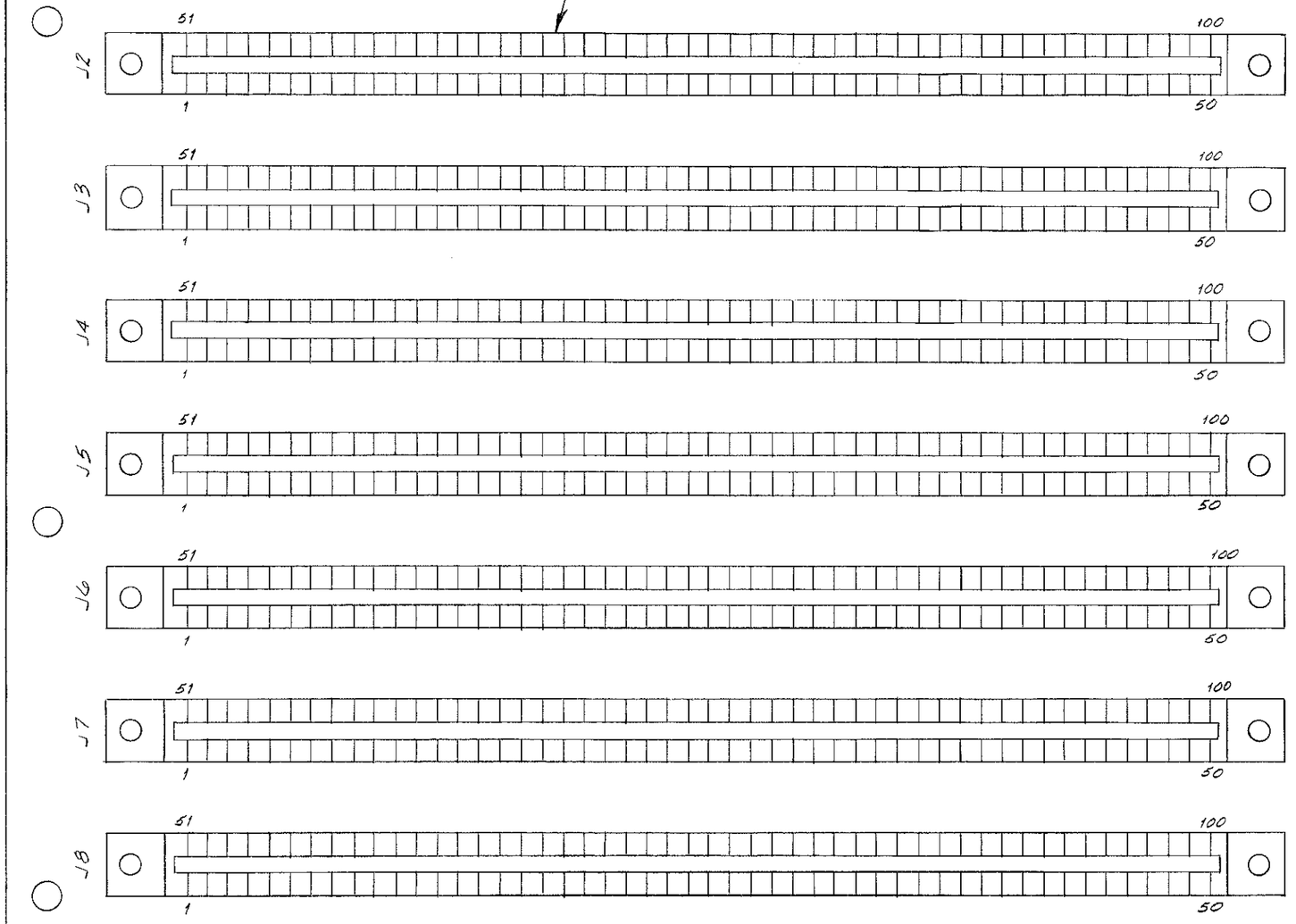
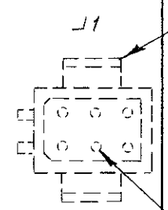


FIGURE 7-17. WIRING DIAGRAM, POWER SUPPLY (SHEET 2)

REVISIONS					
REV	DATE	DESCRIPTION	DFTSMN	ENGR	ECN
A	1-7-83 5-26-83	REVISED & REDRAWN ENGINEERING RELEASE	MERREL		

418-5001
(7 PLCS.)





A17-0677
TO BE MOUNTED ON SOLDER SIDE OF BOARD AFTER WAVE SOLDER.

HEAT AND REMOVE PIN 3 OF J1.

519-0023

TOLERANCE (DECIMAL) U.O.S.
.X ± .030 .XXX ± .005
.XX ± .015 ANGLES ± 1°

DWN. BY	MERREL 1-7-83
CHKD.	
ME	
EE	5-26-83
PROJ. ENGR.	5-26-83
DFTG. SUPVR.	5-26-83 MH
MFG.	

NEXT ASSY.

PRODUCT USED ON
TRANSMITTER CONTROLLER

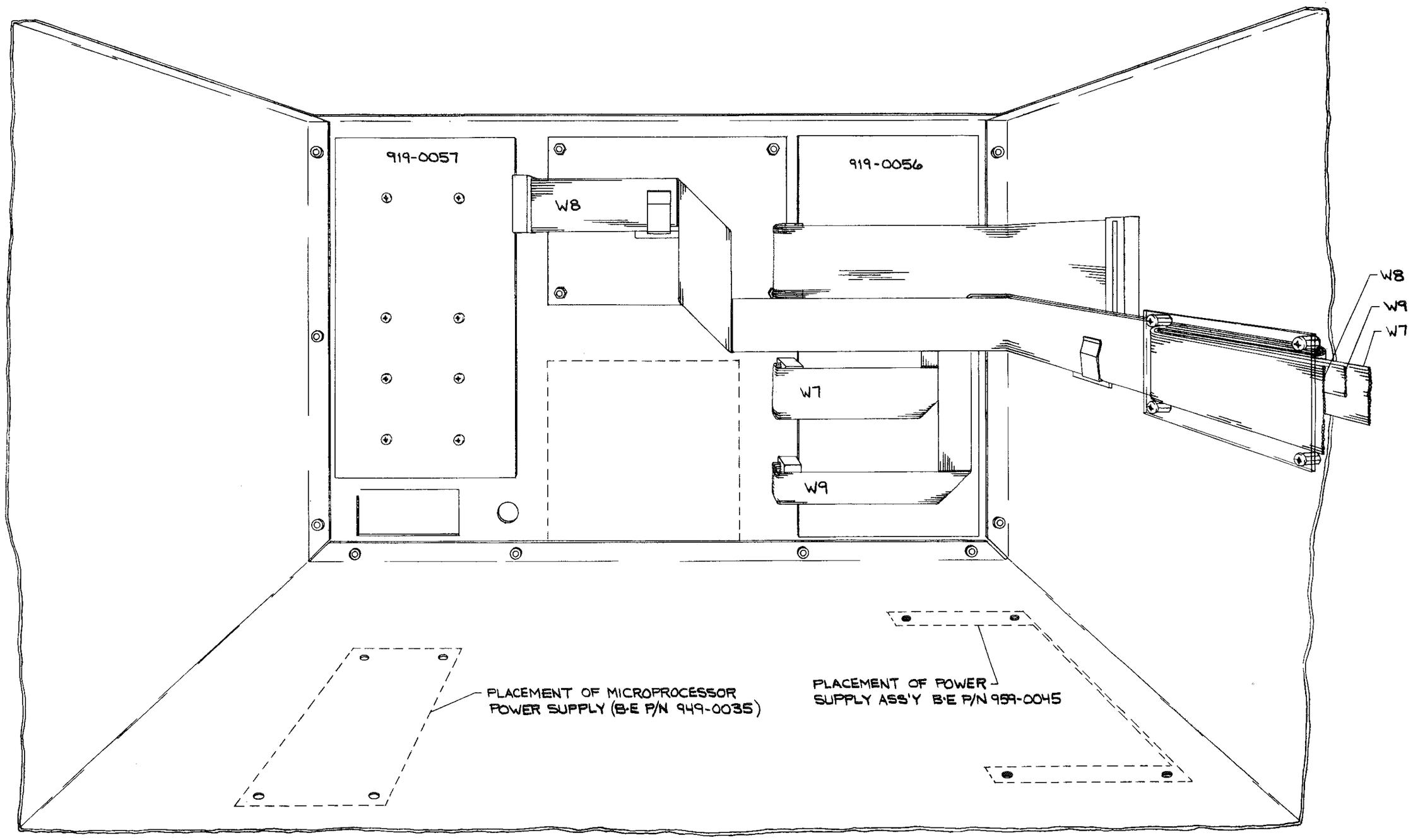
FINISH
———

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST. QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BCST ELECT QUI

TITLE PCB ASSEMBLY-MICROPROCESSOR MOTHERBOARD

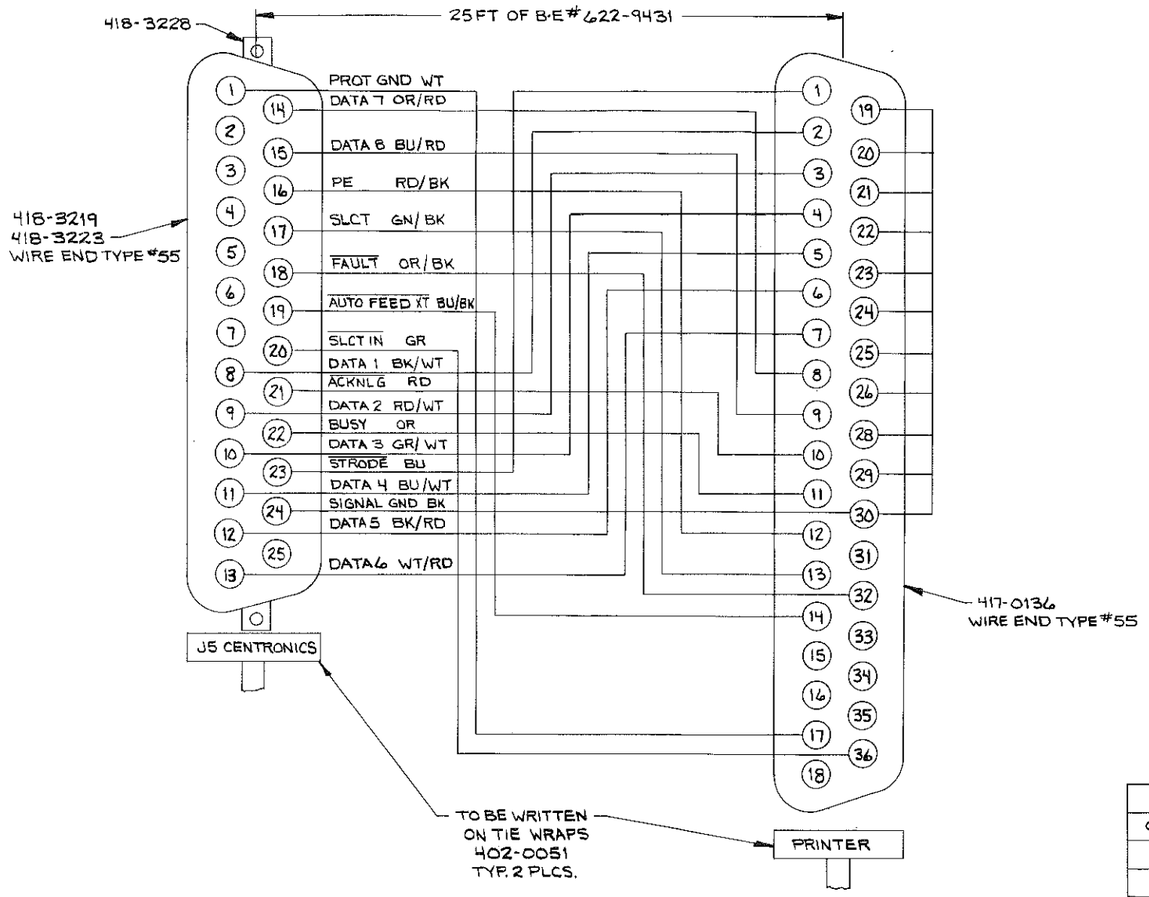
SHEET 1 OF 1
SCALE 2/1
REV A

TYPE A SIZE C DWG. NO. 919-0023



597-0036-24

FIGURE 7-19. ASSEMBLY DIAGRAM, CONTROLLER CABINET RIBBON CABLES



PARTS LIST		
QTY	B·E P/N	DESCRIPTION
1	418-3219	CONNECTOR, 25-PIN
1	417-0136	CONNECTOR, 36-PIN (CENTRONICS)
25 FT	622-9431	CABLE, 20 CONDUCTOR
1	418-3223	CONNECTOR, HOOD
1	418-3228	LOCKING KIT

NOTE:
REMAINING HOLES OF CONNECTOR TO BE FILLED WITH EMPTY PINS

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY JAH 10-3-84
CHKD
ME
PROJ. ENGR.
MFG.

MATERIAL
FINISH
NEXT ASSY.

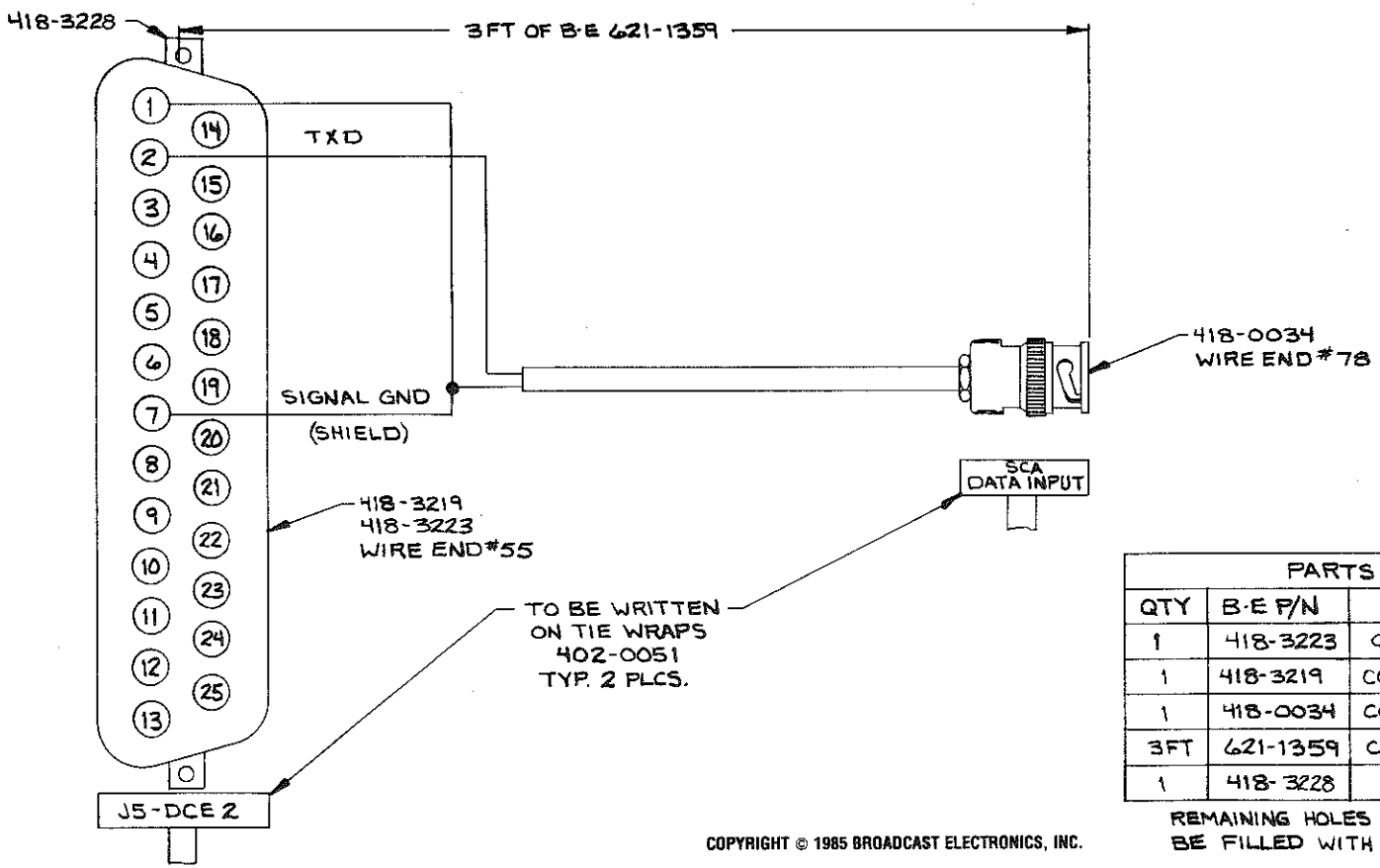
BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE CABLE ASSEMBLY, MVDS LOCAL PARALLEL PRINTER LOGGING

TYPE A | SIZE C | DWG. NO. 949-0110 | REV A

MODEL FM XMTR | SCALE — | SHEET 1 OF 1

REVISIONS					
REV	DATE	DESCRIPTION	DFTSMN	ENGR	ECN



PARTS LIST		
QTY	B-E P/N	DESCRIPTION
1	418-3223	CONNECTOR, HOOD
1	418-3219	CONNECTOR, 25-PIN
1	418-0034	CONNECTOR, BNC
3FT	621-1359	COAX CABLE, RG316U
1	418-3228	LOCKING KIT

REMAINING HOLES OF CONNECTOR TO BE FILLED WITH EMPTY PINS.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY JAH 10-3-84
CHKD
ME
PROJ. ENGR.
MFG.

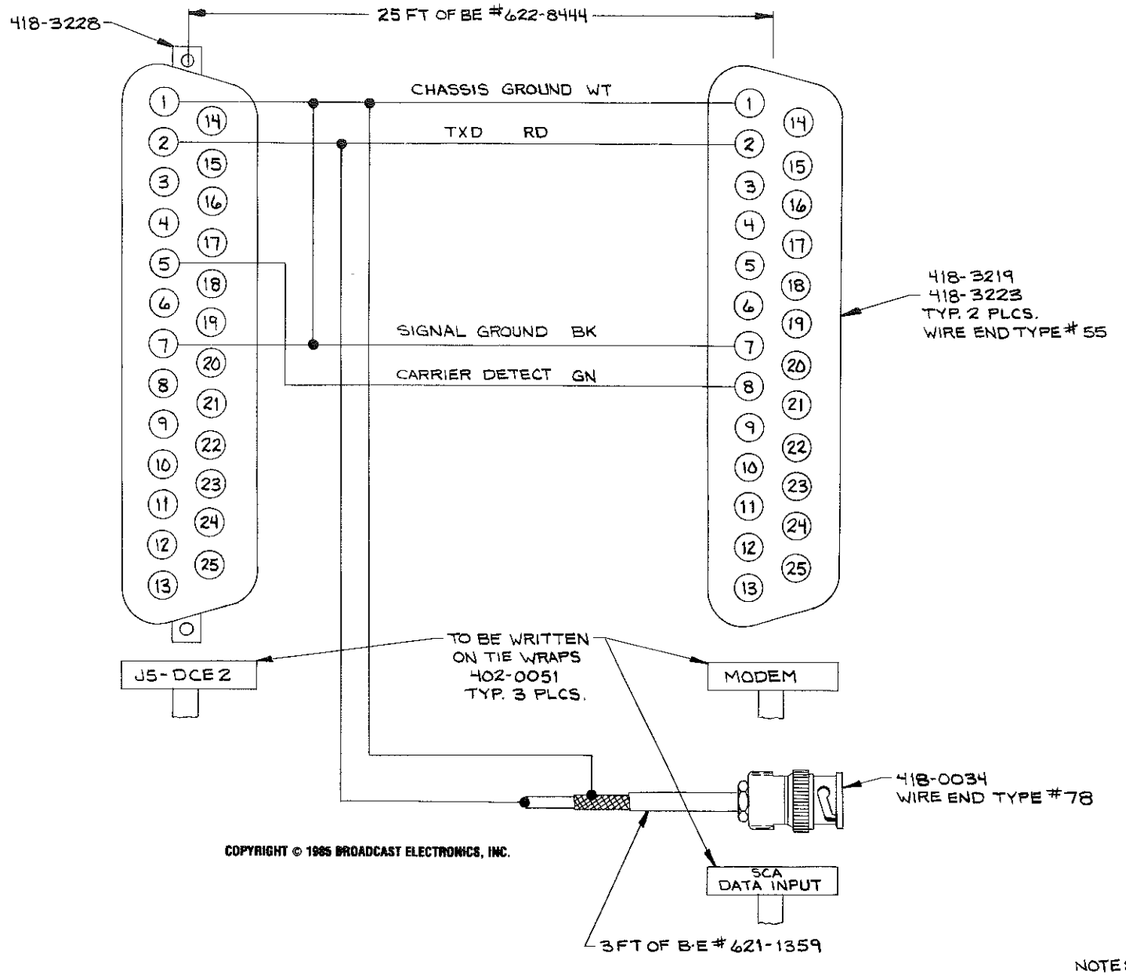
MATERIAL
FINISH
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE CABLE ASSEMBLY, MVDS SCA LOGGING PATH

TYPE A | SIZE B | DWG. NO. 949-0111 | REV A

MODEL FM XMTR | SCALE — | SHEET 1 OF 1



PARTS LIST		
QTY	B-E P/N	DESCRIPTION
2	418-3219	CONNECTOR, 25-PIN
1	418-0034	CONNECTOR, BNC
3FT	621-1359	COAX CABLE RG316
25FT	622-8444	CABLE, 4 CONDUCTOR
2	418-3223	CONNECTOR, HOOD
1	418-3228	LOCKING KIT

NOTE:
REMAINING HOLES OF CONNECTOR TO BE FILLED WITH EMPTY PINS

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY JAH 10-4-84
CHKD
ME
PROJ. ENGR.
MFG.

MATERIAL
FINISH
NEXT ASSY.

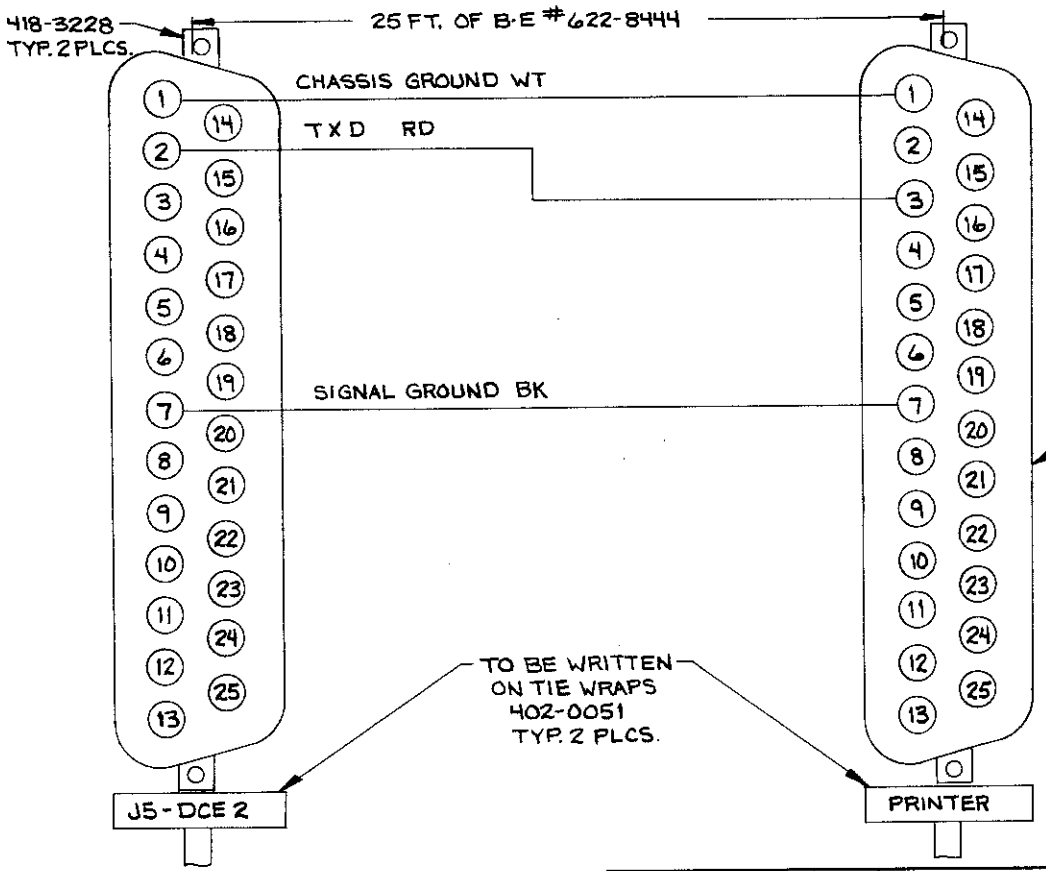
BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE CABLE ASSEMBLY, MVDS MODEM & SCA LOGGING PATHS

TYPE A | SIZE C | DWG. NO. 949-0112 | REV A

MODEL FM XMTR | SCALE — | SHEET 1 OF 1

REVISIONS					
REV	DATE	DESCRIPTION	DFTSMN	ENGR	ECN



PARTS LIST		
QTY	B·E P/N	DESCRIPTION
2	418-3219	CONNECTOR, 25-PIN
25 FT	622-8444	CABLE, 4 CONDUCTOR
2	418-3223	CONNECTOR, HOOD
1	418-3228	LOCKING KIT

FILL REMAINING HOLES WITH EMPTY PINS

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY JAH 10-2-84
CHKD
ME
PROJ. ENGR.
MFG.

MATERIAL
FINISH
NEXT ASSY.

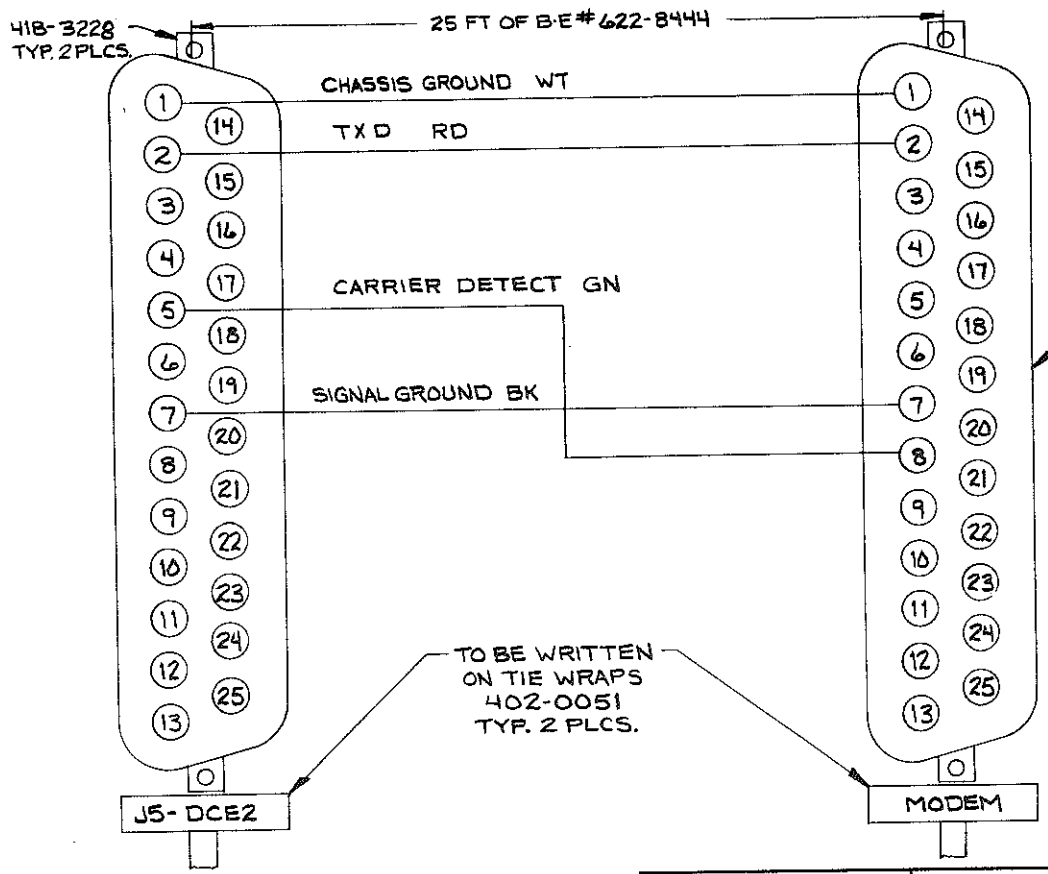
BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE CABLE ASSEMBLY, MVDS LOCAL SERIAL PRINTER LOGGING

TYPE	SIZE	DWG. NO.	REV
A	B	949-0113	A

MODEL FM XMTR SCALE — SHEET 1 OF 1

REVISIONS					
REV	DATE	DESCRIPTION	DFTSMN	ENGR	ECN



PARTS LIST		
QTY	B·E P/N	DESCRIPTION
2	418-3219	CONNECTOR, 25-PIN
25FT	622-8444	CABLE, 4 CONDUCTOR
2	418-3223	CONNECTOR, HOOD
1	418-3228	LOCKING KIT

NOTE:
REMAINING HOLES OF CONNECTOR TO BE FILLED WITH EMPTY PINS

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY JAH 10-3-84
CHKD
ME
PROJ. ENGR.
MFG.

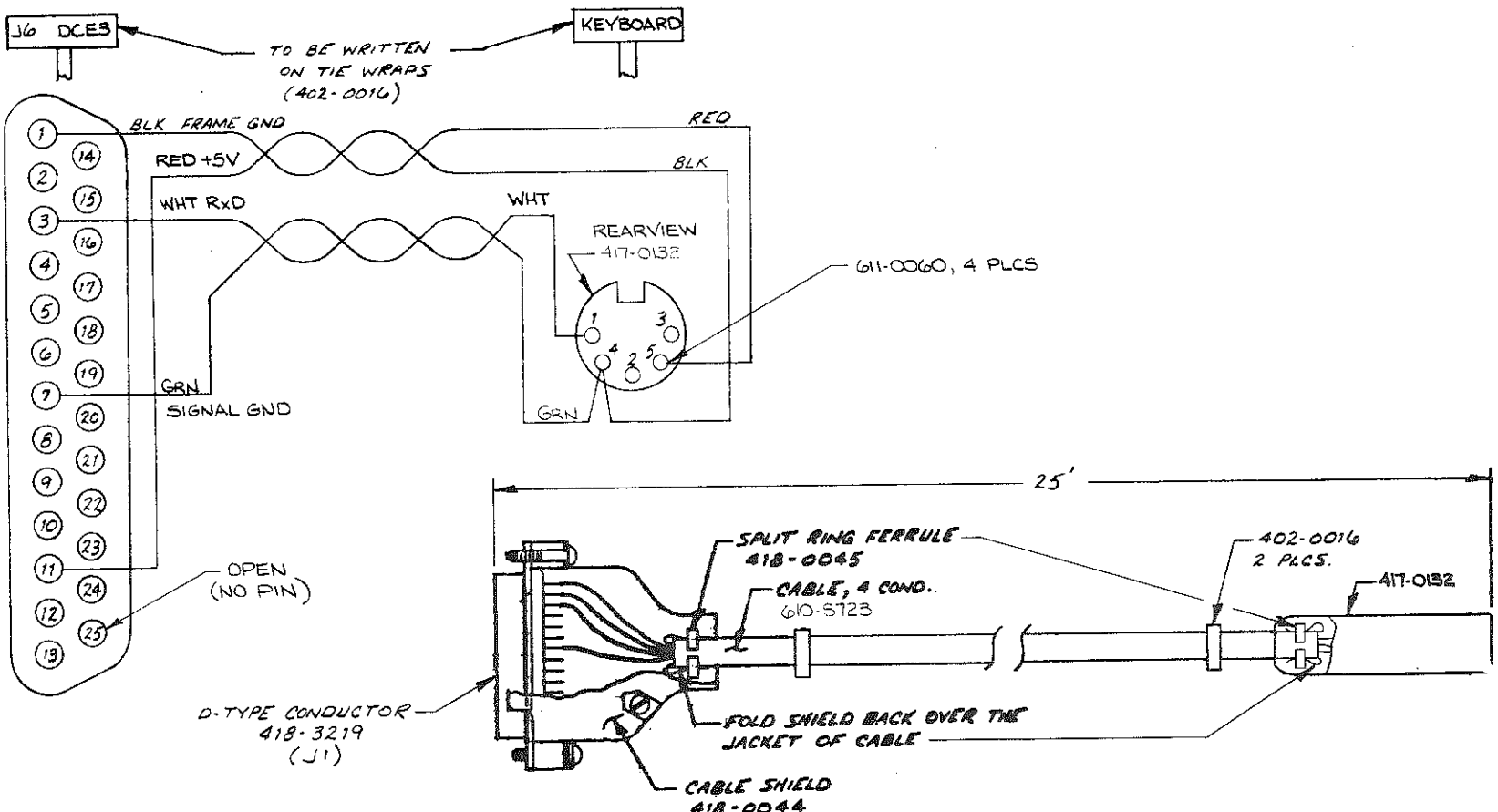
MATERIAL
FINISH
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE CABLE ASSEMBLY, MVDS MODEM LOGGING PATH

TYPE | SIZE B | DWG. NO. 949-0114 | REV A

MODEL FM XMTR | SCALE — | SHEET 1 OF 1



TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1

DWN. BY MSE 6-2-86
CHKD
ME
PROJ. ENGR.
MFG.

MATERIAL —
FINISH
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606 QUINCY, IL 62305 217 224-9500
TELEX 250142 CABLE BROADCAST

TITLE CABLE ASSEMBLY - MVDS TO MICROSWITCH KEYBOARD

TYPE	SIZE	DWG. NO.	REV
A	B	949-0105	H

MODEL | SCALE NL | SHEET 7 OF 8

APPENDIX A

MVDS MANUFACTURERS DATA

A-1. INTRODUCTION.

A-2. This section provides the following technical data relative to the operation and maintenance of the MVDS. Information contained in this section is listed in the following order.

A. Instruction Manual, Sanyo Data Display, VM4509.

B. Instruction Sheet, CRT Video Timer-Controller, CRT 5027.

C. Instruction Sheet, Intel Programmable Communication Interface, 8251A.

D. Instruction Sheet, Zilog Central Processing Unit, Z80.

E. Instruction Sheet, Analog Devices Eight-Bit Eight-Channel DAS, AD7581L.

F. Instruction Sheet, Motorola Real-Time Clock Plus RAM, MC146818.

G. Instruction Sheet, Intel Programmable Peripheral Interface, 8255A.

H. Instruction Manual, Micro Switch Keyboard, 84ST13-1E.

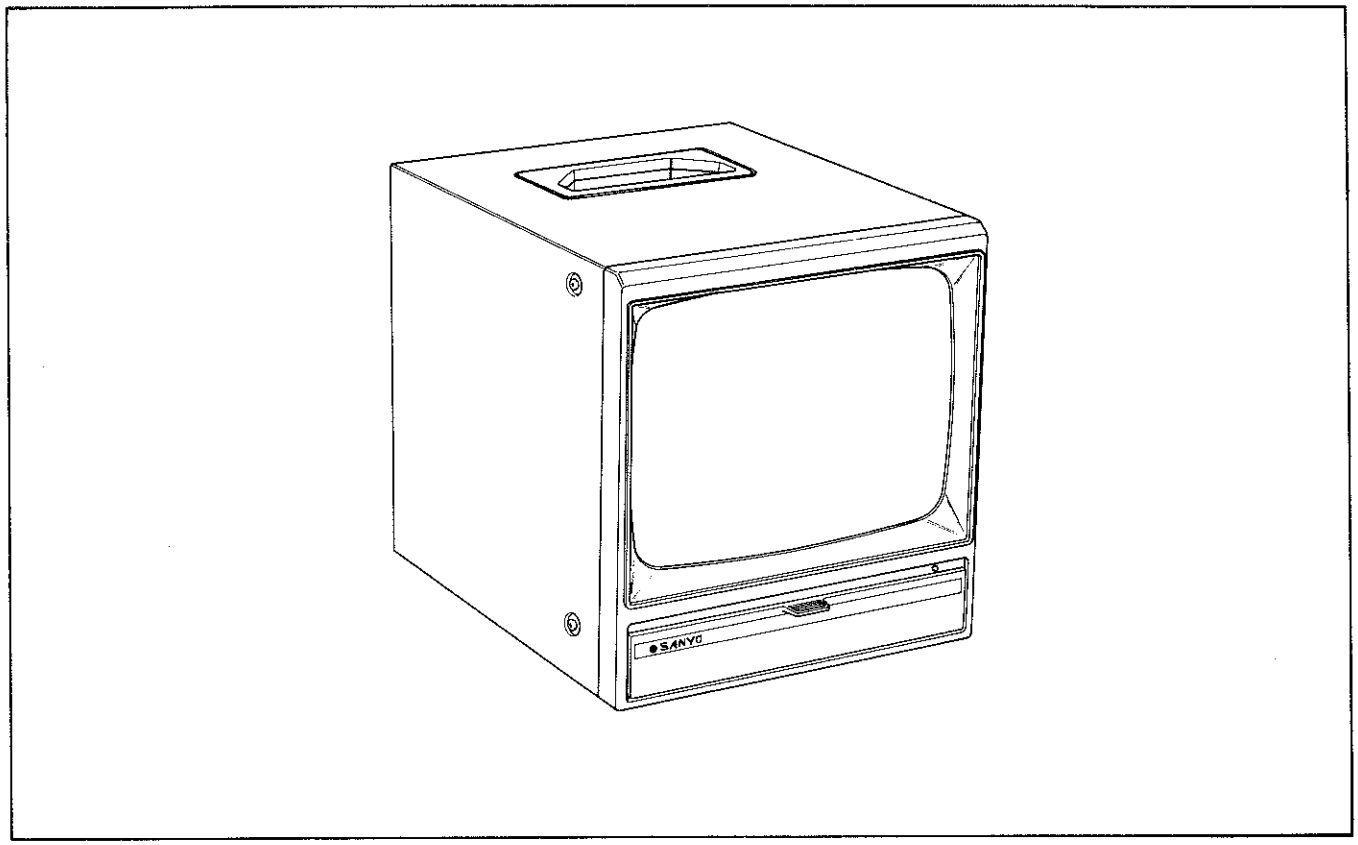
SERVICE MANUAL

SANYO

VIDEO MONITOR

VM4509

(U.S.A.)



SPECIFICATIONS

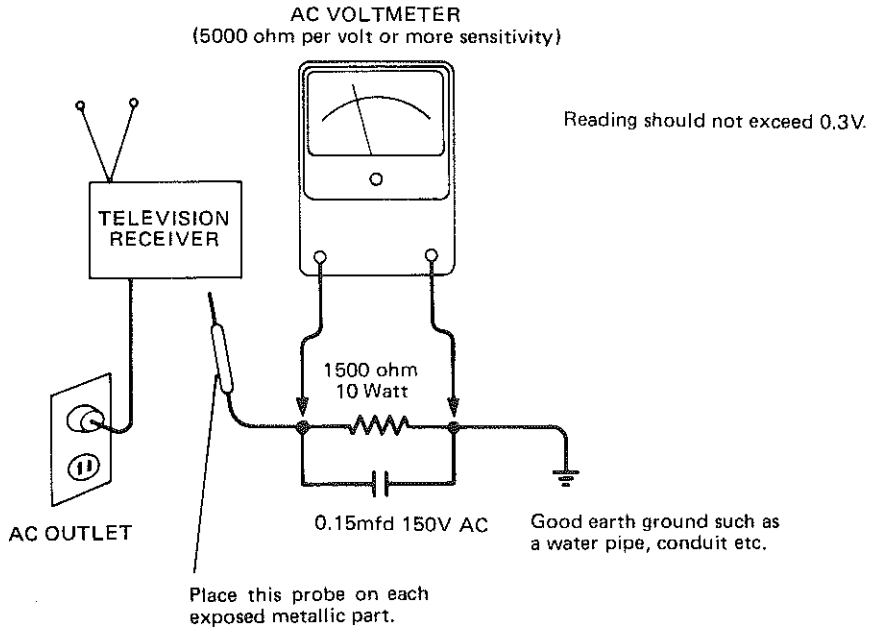
Scanning system	525 lines, 30 frames per sec.
Power source	AC 120 V 60 Hz
Power consumption	AC 33 W, DC 17 W
Picture tube	10-inch diagonal, 90° deflection 240XB4A or 240YB4
Semiconductors	Transistor 13
	Diode 16
Horizontal resolution	more than 600 lines
Cabinet dimension	220mm (W) x 238mm (H) x 266mm (D) approx.
Net weight	5.8 kg approx.
Video	
input signal level	1.0 Vp-p
input impedance	High - 75 ohm switchable
output signal level	0.5 - 1.5 Vp-p
output impedance	over 10K ohm

NOTE: Specifications are subject to change without notice.

SAFETY PRECAUTION

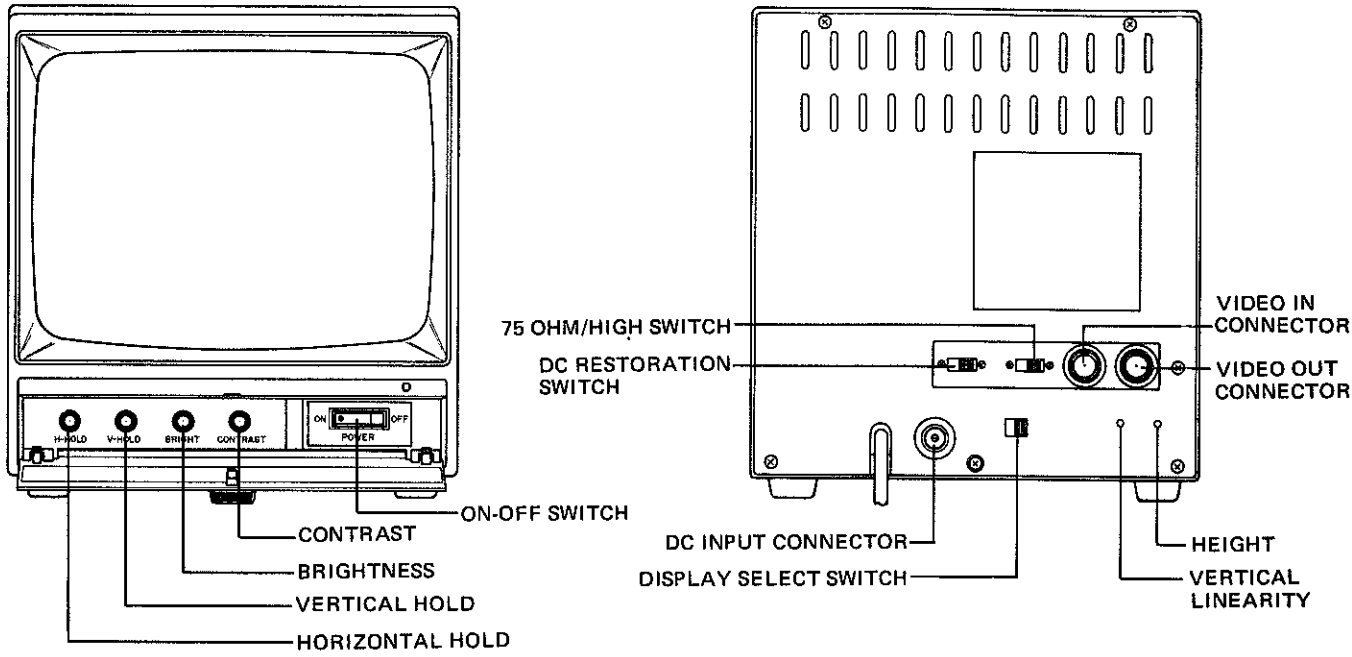
WARNING: Service should not be attempted by anyone unfamiliar with the necessary precautions on this receiver. The following precautions are necessary during servicing.

1. Some parts such as a picture tube in this receiver have special safety-related characteristics for X-RAY RADIATION protection. For continued safety, the parts replacement should be undertaken referring to item 2 below.
2. Many electrical and mechanical parts in this receiver have special safety-related characteristics for protection against shock hazard, fire hazard and others. These characteristics are often passed unnoticed by a visual inspection and the protection afforded by them cannot necessarily be obtained by using replacement components rated for higher voltage wattage, etc. Replacement parts which have these special safety characteristics are identified in this manual and its supplements by shading on the schematic diagram and the parts list. Before replacing any of these components, read the parts list in this manual carefully.
3. When replacing a chassis in the cabinet, always be certain that all the protective devices are installed properly, such as; insulating covers, barriers, strain relief, isolation resistor-capacitor network, etc.
4. Before replacing the back cover of the set, thoroughly inspect inside the cabinet to see that no stray parts or tools have been left inside.
5. Before returning the set to the customer, always perform an AC leakage current check on the exposed metallic parts of the cabinet, such as antennas, terminals, screwheads, metal overlays, control shafts, earphone jack etc. to be sure the set is safe to operate without danger of electrical shock. Plug the AC line cord directly into a 120V AC outlet (do not use a line isolation transformer during this check). Use an AC voltmeter having 5000 ohms per volt or more sensitivity in the following manner:
   Connect a 1500 ohm, 10 watt resistor, paralleled by a 0.15mfd, 150V AC capacitor, between a known good earth ground (water pipe, conduit, etc.) and the exposed metallic parts, one at a time. Measure the AC voltage across the combination of 1500 ohm resistor and 0.15mfd capacitor. Reverse the AC plug at the AC outlet and repeat AC voltage measurements for each exposed metallic part. Voltage measured must not exceed 0.3 volts RMS. This corresponds to 0.2mA AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.



Voltmeter Hook-up for Leakage Current Check

CONTROLS AND TERMINAL IDENTIFICATION



MECHANICAL DISASSEMBLIES

CABINET BACK REMOVAL

1. Carefully lay cabinet face down on soft mat.
2. Remove five(5) screws securing the cabinet back. (See Fig. 1)

CHASSIS REMOVAL

1. First remove the cabinet back and remove four(6 - 9) screws securing the cabinet. (See Fig. 2)
2. Disconnect anode cap, picture tube socket, grounding connector, and LED connector. Then slightly loosen the screw securing the deflection yoke.
3. Remove six(10 - 15) screws. Separate chassis from the escutcheon. (See Fig. 2)

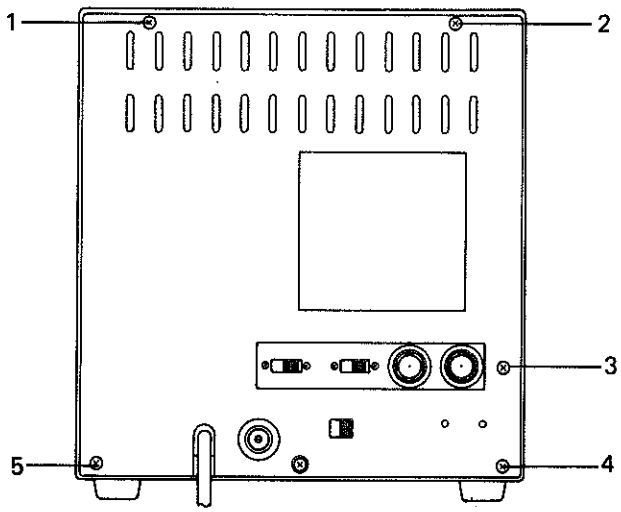


Fig. 1

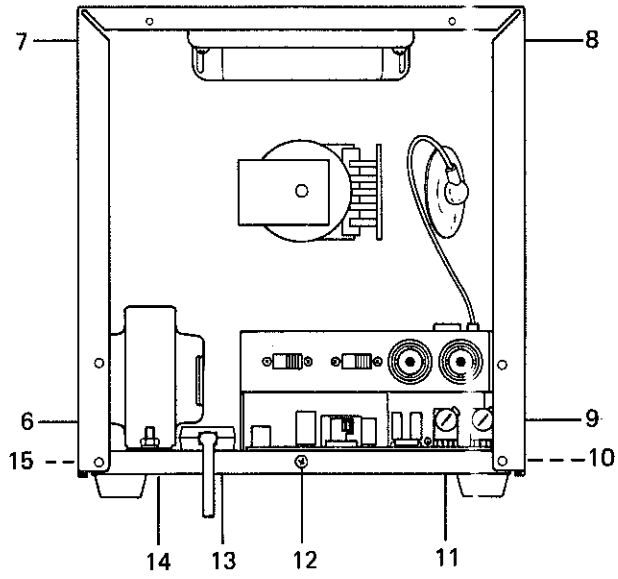


Fig. 2

IMPORTANT NOTICE FOR SERVICE PERSONNEL BEFORE SERVICING

PLEASE READ BEFORE ATTEMPTING SERVICE

1. Line voltage must be kept within ±10% of the rated voltage.
2. When operating at line voltage, confirm the DC voltage at TP1 (J403) is 10.5 ± 0.1V. (Adjust VR701)
3. Keep line voltage when adjusting Horizontal Oscillator or Deflection circuit.
4. When adjusting Horizontal Oscillator Frequency, do not vary this frequency more than ± 800Hz from 15,750Hz center frequency (800Hz equals 13 bars)
5. DO NOT DISCHARGE, ARC, OR MEASURE HIGH VOLTAGE WHEN HIGH VOLTAGE LEAD IS CONNECTED TO CRT. DISCHARGE 2ND ANODE OF CRT ONLY AFTER HIGH VOLTAGE LEAD HAS BEEN DISCONNECTED. DO NOT DISCHARGE HIGH VOLTAGE LEAD AT ANY TIME, DAMAGE TO TRANSISTORS MAY RESULT.
6. While the receiver is in operation, do not attempt to connect or disconnect any wires.
7. Disconnect all power before attempting any repairs.
8. When the power is on, do not attempt to short any portion of the circuit. This shorting may cause damage to the transistors in the receiver.

ADJUSTMENT

PICTURE FOCUS

Adjust focus-VR (VR602) to obtain the best focus. While the adjustment, do not disconnect the picture tube coating earth.

PICTURE WIDTH

1. If picture is too wide, cut the link J605. This connection may have been opened in some chassis as a result of factory adjustment.
2. If picture is still too wide, cut the link J606. (See Fig. 3)

DEFLECTION YOKE AND CENTERING RINGS

1. Loosen the Deflection Yoke clamp and carefully move the yoke on the neck of the picture tube as far foward as possible. Rotate the yoke until the top and bottom edges of the raster are straight. Tighten the clamp.
2. Center the raster and eliminate shaded corners by rotating the centering rings until the best effect is obtained.

VERTICAL HEIGHT AND LINEARITY

PRELIMINARY

1. Adjust AC power to the rated voltage with a voltage regulator.
2. Set V-Hold (VR503), Height (VR502) and V-Linearity (VR501) controls to the mid-position and Contrast (VR201) Brightness (VR202) controls to the fully clockwise.
3. Turn the switch "ON" and leave the receiver for about 5 minutes before proceeding the following adjustments.

ADJUSTMENT PROCEDURE

1. Adjust the V-Linearity control to obtain the best linearity.
2. Adjust the Height control to obtain proper picture height
3. Rotate V-Hold control completely clockwise or counterclockwise to confirm the picture rolls up or down at both extreme positions.

SUB-BRIGHTNESS

1. Set Brightness (VR202) and Contrast (VR201) controls to maximum.
2. Adjust Sub-Brightness control (VR203) to sufficient brightness not exceeding the limit of dim lines produced.

PARTS LOCATION

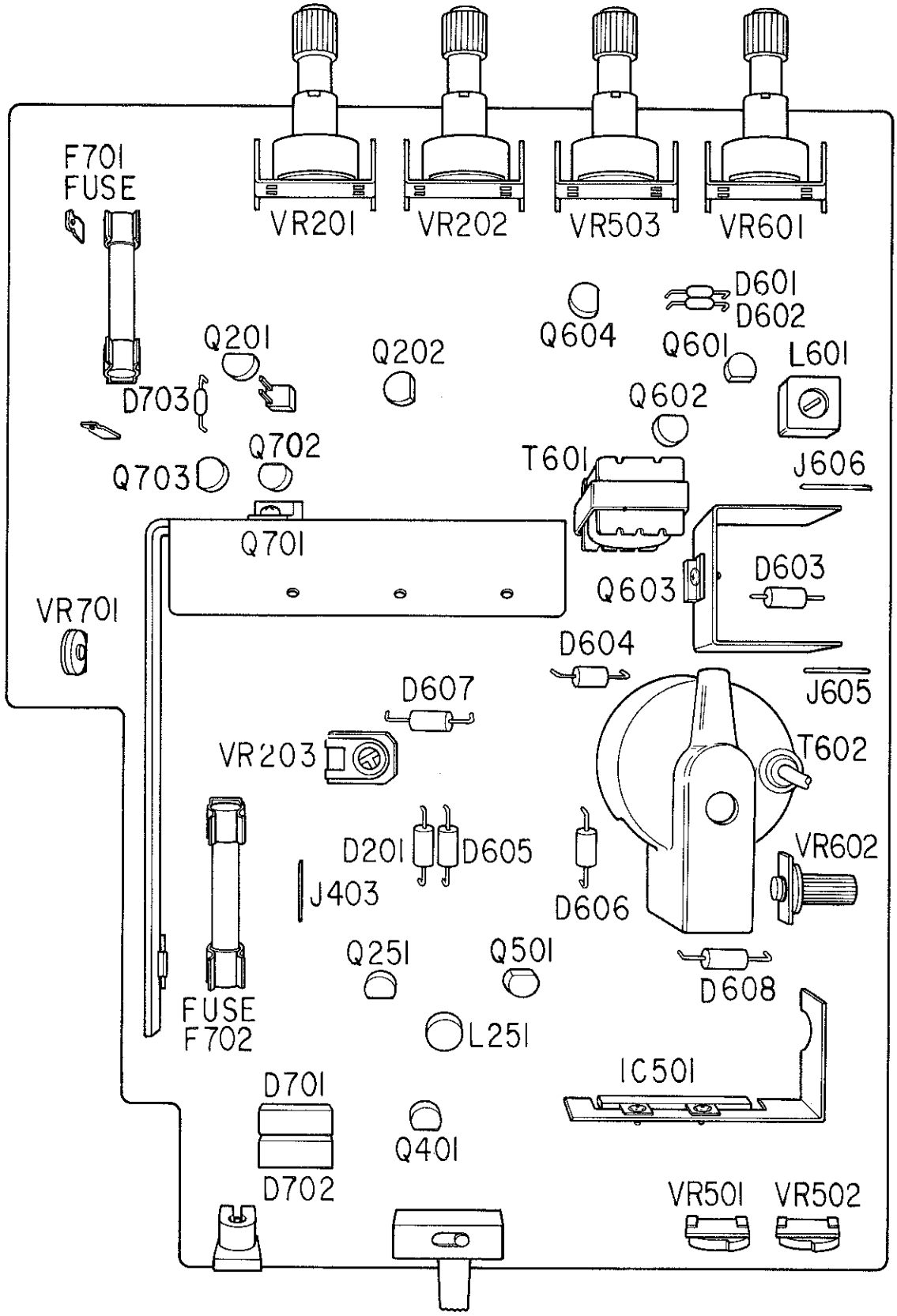
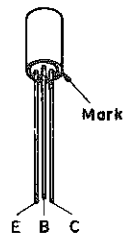
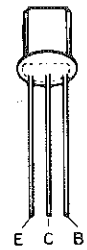
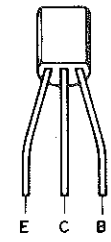
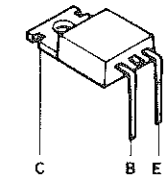
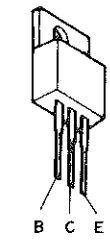
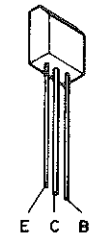
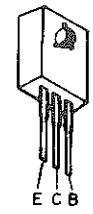
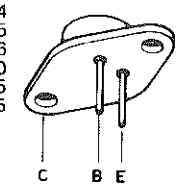
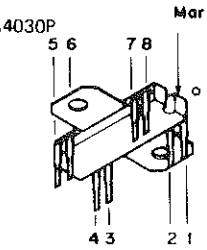
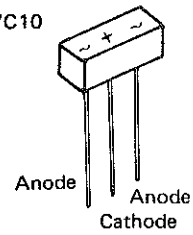
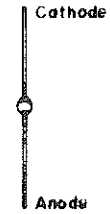
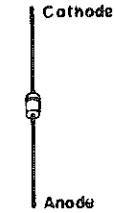
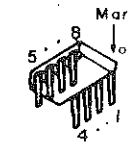
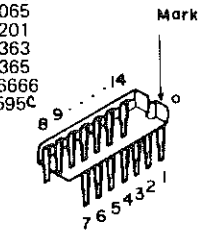
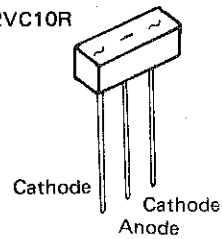
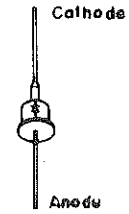
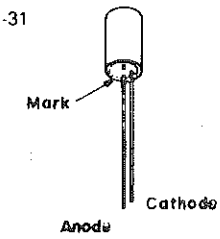
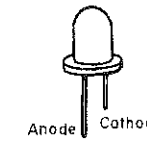
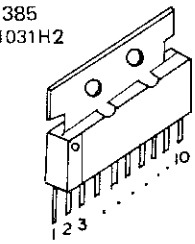


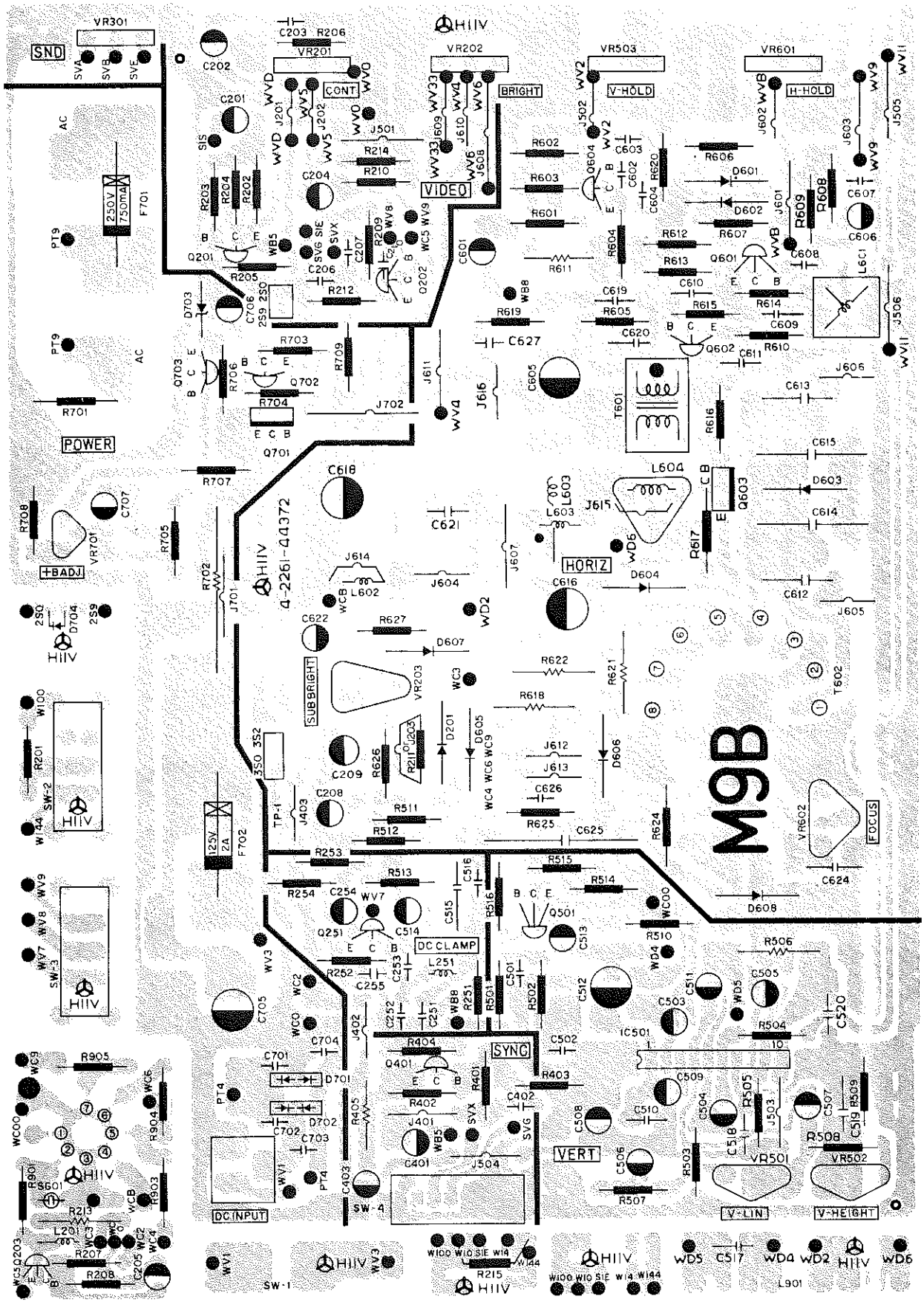
Fig. 3

TERMINAL VIEW

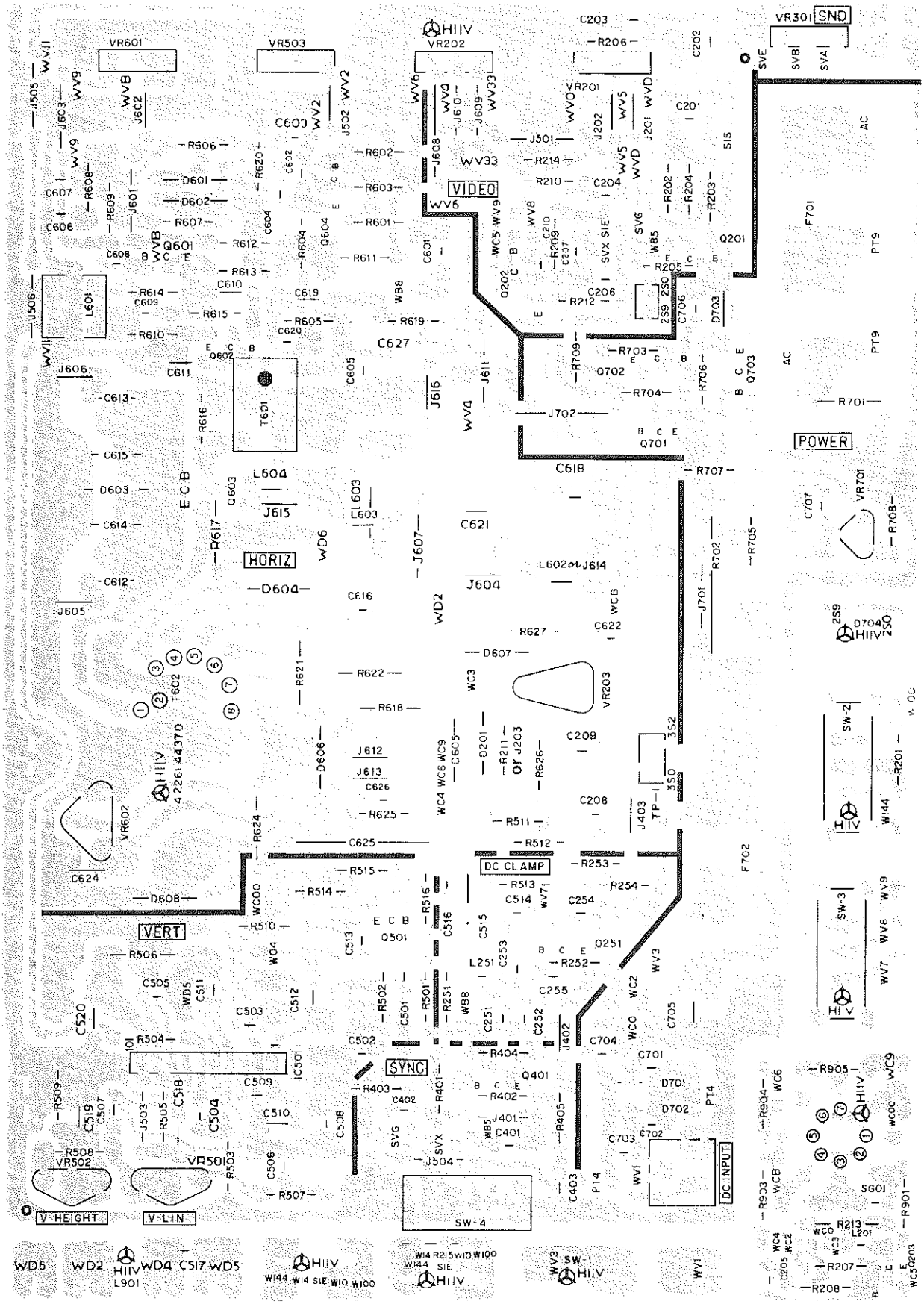
2SA201 2SB187 	2SA495 	2SA608 2SA643 2SA659 2SA733 2SB598 2SC536 2SC929 2SC930 2SC945 2SC1175 2SC1293 2SC2271 2SC2228 2SD400 2SD438 	2SD314 2SD331 	2SB507 2SB511 2SC1096 2SC1506 2SC1507 2SC1520 2SC1755 2SC1756 2SC2373 2SD823 2SD313 2SD325 2SD386 
2SC983 2SC1941 	2SD612 	2SB375 2SB407 2SB474 2SC1024 2SC1025 2SC1046 2SC1050 2SC1295 2SC1875 2SD24 2SD315 2SD353 2SD575 2SD627 2SC1892 	2SC2057 	LA4030P 
S2VC10 	1JZ61 1R5TH61 ERB30-15 ERC27-13 V09G 	1S188 1S553 1S1005 1S1834 1S2076 1SS81 BZ-110 ERB-24-02D SIB01-02 SM-1-02FR RD7.5E RD11F W09C WZ-063 WZ-075 WZ-110 ERB24-06D 	LA1354 uPC596C 	LA1352 CA3065 LA1201 LA1363 LA1365 SN76666 uPC595C 
S2VC10R 	DS-113 	SV-31 	SLP-131B 	LA1385 uPC1031H2 

E : Emitter C : Collector B : Base S : Shield

CIRCUIT BOARD DIAGRAM



CIRCUIT BOARD DIAGRAM



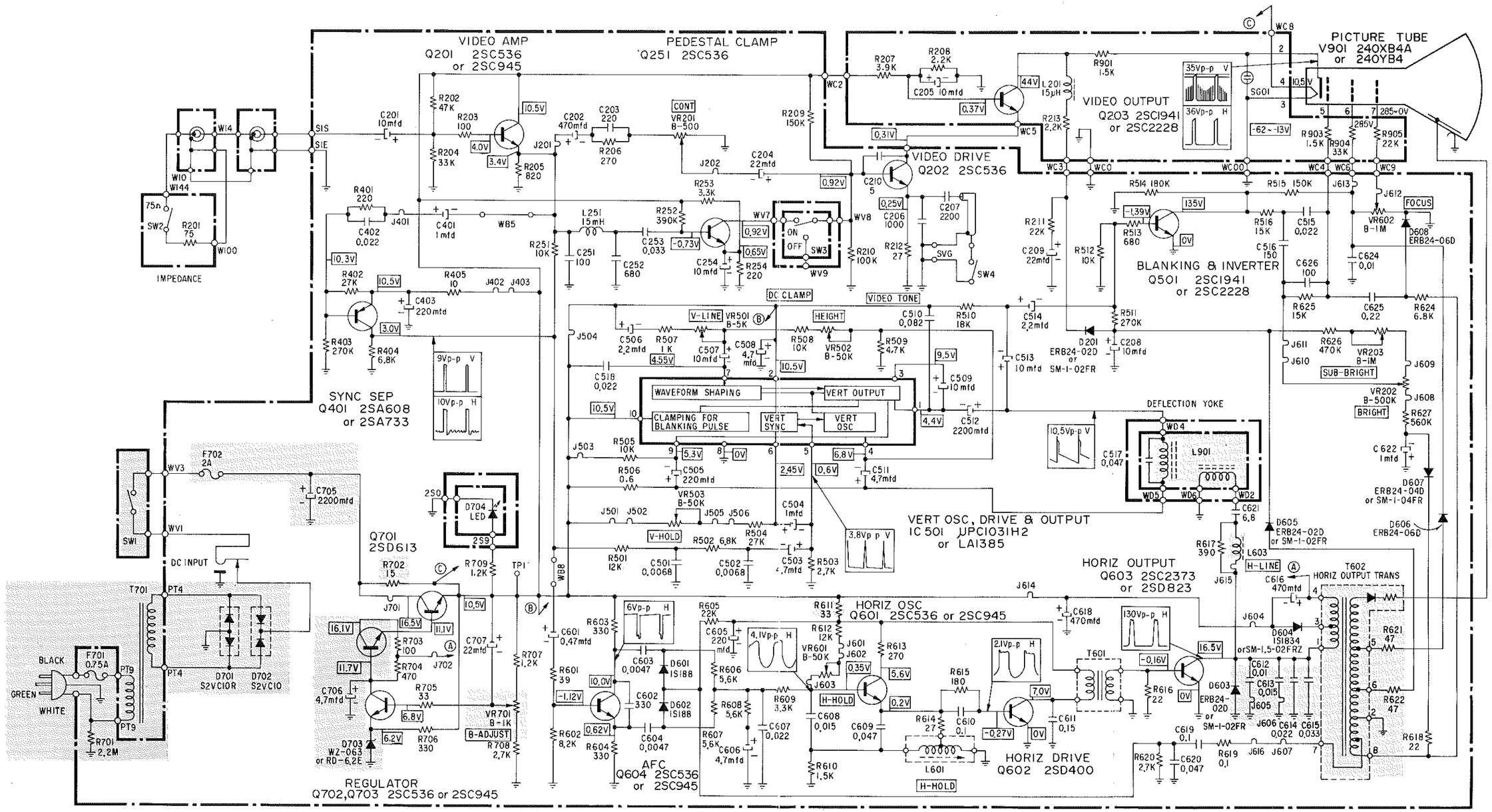
SCHEMATIC DIAGRAM

PRODUCT SAFETY NOTICE

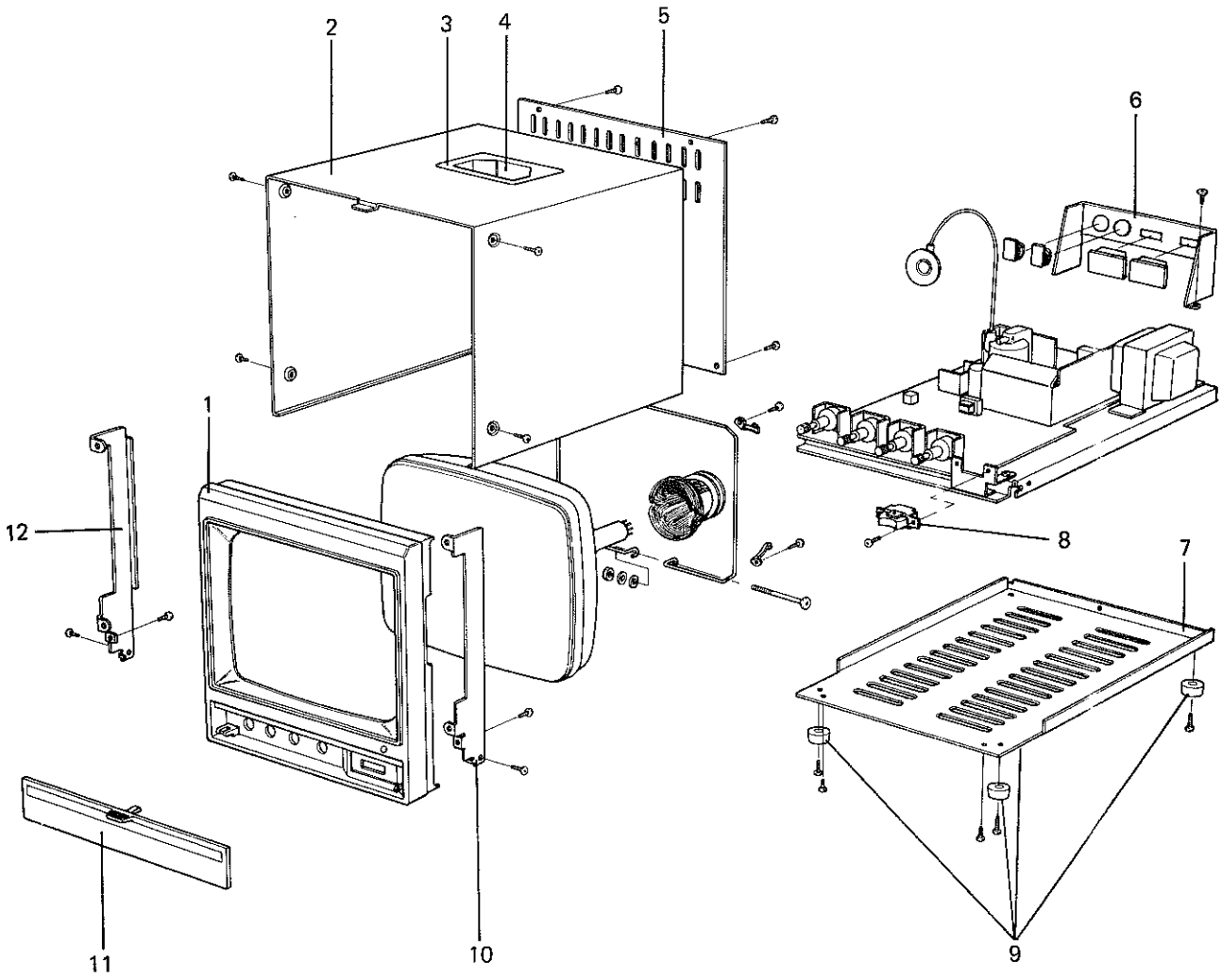
The shaded areas of this schematic diagram designate components whose value and tolerance are of special significance to product safety. Should the components in the shaded areas need to be replaced, only parts designated on the parts list are to be used. No deviations from resistance, wattage and voltage rating may be made for replacement items in the shaded areas.

NOTES:

1. All resistance values in ohm.
   K = 1,000 M = 1,000,000
2. Unless otherwise noted in schematic diagram, all capacitors less than 1 are expressed in mfd, and the values larger than 1 are in pF.
3. Voltage reading taken with "VTVM" from point indicated to chassis ground, tuner on unused channel, contrast at max., other controls at normal, local line voltage.
4. All waveformes measured with strong signal input, contrast set to give normal picture.
5. Voltage reading may vary ±20%.
6. This is a fundamental circuit diagram. Some production changes may be made without revision of the diagram.



REPLACEMENT PARTS LIST



Key No.	Parts No.	Description	Q'ty
1	111 0 1211 08970	ESC ASSY-MAT-V0	1
2	111 2 1111 12070	CABINET-MAT	1
3	111 2 1711 23570	HANDLE TOP-MAT-V0	1
4	111 2 1711 23670	HANDLE BOTTOM-MAT-V0	1
5	111 2 1171 26570	BACK COVER-MAT	1
6	111 2 3651 22070	CONN MAG BRKT-MAT	1
7	111 2 1181 12770	BOTTOM COVER-MAT	1
8	4 2311 05272	SEESAW SWITCH	1
9	111 2 1731 11270	FEET-MAT	4
10	111 2 3311 23170	R CHAS MTG BRKT-MAT	1
11	111 0 1371 04870	DOOR ASSY-MAT	1
12	111 2 3311 23270	L CHAS MTG BRKT-MAT	1

PARTS LIST

PRODUCT SAFETY NOTICE

PRODUCT SAFETY SHOULD BE CONSIDERED WHEN A COMPONENT REPLACEMENT IS MADE IN ANY AREA OF A RECEIVER. THE SHADED AREAS OF THIS PARTS LIST AND THE SCHEMATIC DIAGRAM DESIGNATE COMPONENTS IN WHICH SAFETY CAN BE OF SPECIAL SIGNIFICANCE. IT IS PARTICULARLY RECOMMENDED THAT ONLY PARTS DESIGNATED ON THE FOLLOWING PARTS LIST BE USED FOR COMPONENT REPLACEMENT IN THE SHADED AREAS. REFER TO PAGE 2 OF THIS MANUAL. NO DEVIATIONS FROM RESISTANCE, WATTAGE, OR VOLTAGE TOLERANCE MAY BE MADE FOR REPLACEMENT ITEMS IN SHADED AREAS.

Schematic Location	Parts No.	Description	Q'ty
CHASSIS PARTS			
	111 0 6211 06070	POWER RAD PL AY-MAT	1
	111 2 3121 18770	CHASSIS FRAME-MAT	1
	111 2 3651 22070	CONN MTG BRKT-MAT	1
	111 2 3691 16570	SW MTG BRKT-MAT	1
	111 2 5291 12870	FBT HOLD BRKT-MAT	1
	111 2 6211 22670	HOR RAD PLATE-TJJ	1
	111 2 6211 22770	VERT RAD PLATE-TJJ	1
	111 2 6221 14170	M CONN EARTH TIP-MAT	1
	111 2 7211 14171	WIRE HOLDER-MAJ-V0	1
PACKING MATERIALS			
	111 6 1421 59970	IND CORR CASE-MAT	1
	111 6 2611 20870	IND POLY COVER-MAT	1
	111 6 3111 55370	TOP INNER CUSH-MAT	1
	111 6 3111 55470	BOT INNER CUSH-MAT	1
	111 6 3231 12170	PROTECT SHEET-MAT	1
ACCESSORIES AND LABELS			
	111 2 7141 12770	CAUTION LABEL-ZL-A	1
	111 2 7161 10570	UL LABEL-M	1
	111 6 2701 15000	PM ASSY-MAT	1
	111 6 2711 05770	ENVELOPE-SR-B	1
	111 6 4111 99570	INST MANUAL-MAT	1
	111 6 4511 13671	REGISTRATION CARD-M	1
	111 6 4511 14871	WARRANTY CARD-US-M-D	1
	111 6 4151 18370	SAFETY TIPS-MAJ	1
	111 6 4511 14570	WARRANTY CARD-US-M-B	1
	111 6 4551 18370	SERIAL NO LABEL-US	1
	111 6 4551 19070	HEW SERIAL CARD-INC	1
	111 6 4721 14970	CAUTION LABEL-TCD-B	1
	111 6 4721 16570	CAUTION LABEL-MAD	1
	111 6 4721 19470	HEW NOTICE	1
	111 6 4721 21970	FBT WARNING LABEL-H	1
	111 6 4721 27570	FUSE CAU LABEL-MAT	1
	111 6 4721 27970	CAUTION LABEL-MAT	1
	111 6 4751 14070	CRT BRAND LABEL-SA	1
	111 6 4751 15970	CRT LABEL 240XB4A-B	1
	111 6 4761 32970	SPEC LABEL-MAT	1
	111 6 4761 32971	SPEC LABEL MAT-B	1
	111 6 4761 32972	SPEC LABEL-MAT-C	1
	111 6 4761 33170	SW IND LABEL-MAT	1
SCREWS-CABINET			
		SBT 1, 3.0X 10.C2	4
		SBT , 3.0X 8.Z1	7
		SBT , 3.0X 10.Z1	9
		SBT , 4.0X 12.Z1	9
SCREWS-CHASSIS			
		SNB , 2.6X 4.Z1	4
		STR , 4.0X 12.Z1	2
		SBT , 3.0X 6.Z1	2
		SBT , 3.0X 8.Z1	6
		SBT , 3.0X 16.Z1	2
		SBT , 3.5X 8.Z1	2
		SBW , 4.0.RB	2
		SBW , 4.0X10.0X08Z1	2
		ZRN 1, 4.0.	2
ELECTRICAL PARTS			
L201	4 2531 04771	FILTER COIL	1
L251	4 2531 14270	FILTER COIL 15MH	1
L601	4 2731 06170	HORIZ OSC COIL	1
L603	4 2741 05370	LINEARITY COIL	1
L901	4 2761 50670	DEFLECTION YOKE	1
T601	4 2731 06270	HORIZ DRIVE TRANS	1
T602	4 2751 51300	FLYBACK TRANS	1
T701	4 2511 43012	POWER TRANS	1
SMALL PARTS			
	114 9 1720 10420	MAIN PCB ASSY-MAT-US	1
	4 2261 44370	PC BOARD M9B	1
	4 2311 05272	SEESAW SWITCH	1
	4 2311 07470	SLIDE SWITCH	2
	4 2311 09170	SLIDE SWITCH	1
	4 2350 61600	TERMINAL SOCKET	1
	4 2351 05470	CRT SOCKET	1
	4 2351 44170	FUSE CLIP	4
	4 2351 66470	M-CONNECTER FEMALE	2
	4 2351 74270	1P DC JACK-U	1
	4 2361 05570	GT PIN	1
	4 2361 12270	2P MICRO PLUG	1
	4 2361 14670	1P MICRO PLUG	4
	111 0 9081 02023	2P MICRO SOCKET ASSY	1
	111 0 9131 08824	AC CORD	1
	111 2 6221 11370	1P TERMINAL	2
F701	4 2341 09570	FUSE 0.75A 250V UL	1
F702	4 2341 08270	FUSE 2A 125V UL	1
SG01	4 2341 06270	SPARK GAP	1
or	4 2341 07770	SPARK GAP	1
VARIABLE RESISTORS			
VR201	4 2221 35670	16FRN25ZB-500PK	1
VR202	4 2221 35870	16FRN25ZB-500KPK	1
VR203	4 2221 34770	9C2VFRB-1M	1
VR501	4 2221 35470	12CFR4B-5K	1
VR502	4 2221 35570	12CFR4B-50K	1
VR503	4 2221 35770	16FRN25ZB-50KPK	1
VR601	4 2221 35770	16FRN25ZB-50KPK	1
VR602	4 2221 35070	15CHFR7B-1M	1
VR701	4 2221 29470	8PFRB-1K	1
CAPACITORS			
C201		ELECT 10M 16V	1
C202		ELECT 470M 10V	1
C203		CERAMIC 220P W 50V	1
C204		ELECT 22M 10V	1
C205		ELECT 10M 16V	1
C206		CERAMIC 1000P W 50V	1
C207		CERAMIC 2200P W 50V	1
C208		ELECT 10M 100V	1
C209		ELECT 22M 100V	1
C210		CERAMIC 5P RH 50V	1
C251		CERAMIC 100P SL 50V	1
C252		CERAMIC 680P W 50V	1
C253		MYLAR 0.033M 50V	1
C254		ELECT 10M 16V	1
C401		ELECT 1M 50V	1
C402		MYLAR 0.022M 50V	1
C403		ELECT 220M 16V	1
C501		MYLAR 0.0068M 50V	1
C502		MYLAR 0.0068M 50V	1
C503		ELECT 4.7M 25V	1
C504		TANTAL 1M 25V	1
C505		ELECT 220M 16V	1
C506		ELECT 2.2M 50V	1
C507		ELECT 10M 16V	1

NOTICE: 1. Parts orders must contain Model Number, Parts Number and Description.
2. Ordering quantity of resistors, capacitors and screws must be multiple of 10pcs.
3. Component parts indicated by parentheses in the column Q'ty are not available.

PARTS LIST

Schematic Location	Parts No.	Description	Q'ty
C508		ELECT 4.7M 25V	1
C509		ELECT 10M 16V	1
C510		MYLAR 0.082M 50V	1
C511		TANTAL 4.7M 16V	1
C512		ELECT 2200M 10V	1
C513		ELECT 10M 16V	1
C514		ELECT 2.2M 50V	1
C515		POLYPR 0.022M 400V	1
C516		CERAMIC 150P W 500V	1
C517		MYLAR 0.047M 50V	1
C518		MYLAR 0.022M 50V	1
C601		ELECT 0.47M 50V	1
C602		CERAMIC 330P W 50V	1
C603		MYLAR 0.0047M 50V	1
C604		MYLAR 0.0047M 50V	1
C605		ELECT 220M 16V	1
C606		ELECT 4.7M 25V	1
C607		MYLAR 0.022M 50V	1
C608		POLYPR 0.015M 100V	1
C609		MYLAR 0.047M 50V	1
C610		MYLAR 0.1M 50V	1
C611		MYLAR 0.15M 50V	1
C612		POLYPR 0.01M 400V	1
or		POLYPR 0.01M 630V	1
C613		POLYPR 0.015M 400V	1
C614		POLYPR 0.022M 400V	1
C615		POLYPR 0.033M 400V	1
C616		ELECT 470M 10V	1
C618		ELECT 470M 16V	1
C619		MYLAR 0.1M 50V	1
C620		MYLAR 0.047M 50V	1
C621		ELECT 6.8M 25V	1
C622		ELECT 1M 160V	1
C624		CERAMIC 0.01M Z 500V	1
C625		POLYPR 0.22M 400V	1
C626		CERAMIC 100P W 500V	1
C705		ELECT 2200M 25V	1
C706		TANTAL 4.7M 25V	1
C707		ELECT 22M 16V	1
FIXED RESISTORS			
R201		CARBON 75 1/4WJ	1
R202		CARBON 47K 1/4WJ	1
R203		CARBON 100 1/4WJ	1
R204		CARBON 33K 1/4WJ	1
R205		CARBON 820 1/4WJ	1
R206		CARBON 270 1/4WJ	1
R207		CARBON 3.9K 1/4WJ	1
R208		CARBON 2.2K 1/4WJ	1
R209		CARBON 150K 1/4WJ	1
R210		CARBON 100K 1/4WJ	1
R211		CARBON 22K 1/4WJ	1
R212		CARBON 27 1/4WJ	1
R213		OXIDE-M 2.2K 2WJ	1
R251		CARBON 10K 1/4WJ	1
R252		CARBON 390K 1/4WJ	1
R253		CARBON 3.3K 1/4WJ	1
R254		CARBON 220 1/4WJ	1
R401		CARBON 220 1/4WJ	1
R402		CARBON 27K 1/4WJ	1
R403		CARBON 270K 1/4WJ	1
R404		CARBON 6.8K 1/4WJ	1
R405		CARBON 10 1/4WJ	1
R501		CARBON 12K 1/4WJ	1
R502		CARBON 6.8K 1/4WJ	1
R503		CARBON 2.7K 1/4WJ	1
R504		CARBON 27K 1/4WJ	1
R505		CARBON 10K 1/4WJ	1
R506		OXIDE-M 0.6 1WJ	1
R507		CARBON 1K 1/4WJ	1
R508		CARBON 10K 1/4WJ	1
R509		CARBON 4.7K 1/4WJ	1
R510		CARBON 18K 1/4WJ	1
R511		CARBON 270K 1/4WJ	1
R512		CARBON 10K 1/4WJ	1
R513		CARBON 680 1/4WJ	1
R514		CARBON 180K 1/4WJ	1
R515		CARBON 150K 1/4WJ	1
R516		CARBON 15K 1/4WJ	1
R601		CARBON 39 1/4WJ	1
R602		CARBON 8.2K 1/4WJ	1
R603		CARBON 330 1/4WJ	1
R604		CARBON 330 1/4WJ	1
R605		CARBON 22K [illegible]/4WJ	1
R606		CARBON 5.6K 1/4WJ	1
R607		CARBON 5.6K 1/4WJ	1
R608		CARBON 5.6K 1/4WJ	1
R609		CARBON 3.3K 1/4WJ	1
R610		CARBON 1.5K 1/4WJ	1
R611		CARBON 33 1/4WJ	1
R612		CARBON 12K 1/4WJ	1
R613		CARBON 270 1/4WJ	1
R614		CARBON 27 1/4WJ	1
R615		CARBON 180 1/4WJ	1
R616		CARBON 22 1/4WJ	1
R617		SOLID 390 1/2WK	1
R618		SOLID 22 1/2WK	1
R619		CARBON 1.5K 1/4WJ	1
R620		CARBON 2.7K 1/4WJ	1
R621		SOLID 47 1/2WK	1
R622		SOLID 47 1/2WK	1
R624		SOLID 6.8K [illegible]/2WK	1
R625		CARBON 15K [illegible]/4WJ	1
R626		CARBON 470K 1/4WJ	1
R627		CARBON 560K 1/4WJ	1
R701		SOLID 2.2M 1/2WK	1
R702		WIRE-W 15 7WJ	1
R703		CARBON 100 1/4WJ	1
R704		CARBON 470 1/4WJ	1
R705		CARBON 33 1/4WJ	1
R706		CARBON 330 1/4WJ	1
R707		CARBON 1.2K 1/4WJ	1
R708		CARBON 2.7K 1/4WJ	1
R709		CARBON 1.2K 1/4WJ	1
R901		CARBON 1.5K 1/4WJ	1
R903		CARBON 1.5K 1/4WJ	1
R904		CARBON 33K 1/4WJ	1
R905		CARBON 22K 1/4WJ	1
TUBES AND SEMICONDUCTORS			
D201		SI DIODE ERB24-02D	1
or		SI DIODE SM-1-02FR	1
D601		GE DIODE 1S188TV	1
D602		GE DIODE 1S188TV	1
D603		SI DIODE ERB24-02D	1
or		SI DIODE SM-1-02FR	1
D604		SI DIODE 1S1834	1
or		SI DI SM-1.5-02FRZ	1
D605		SI DIODE ERB24-02D	1
or		SI DIODE SM-1-02FR	1
D606		SI DIODE ERB24-06D	1
D607		SI DIODE ERB24-04D	1
or		SI DIODE SM-1-04FR	1
D608		SI DIODE ERB24-06D	1
D701		SI DIODE S2VC10R	1
D702		SI DIODE S2VC10	1
D703		ZE DIODE WZ-063	1
or		ZE DIODE RD6.2E	1
D704		LED SLP-131B	1
IC501		IC-UPC1031H2	1
or		IC-LA1385	1
Q201		SI TR 2SC536	1
or		SI TR 2SC945	1
Q202		SI TR 2SC536	1
Q203		SI TR 2SC2228	1
or		SI TR 2SC1941	1
Q251		SI TR 2SC536	1
Q401		SI TR 2SA608	1
or		SI TR 2SA733	1
Q501		SI TR 2SC2228	1

NOTICE: 1. Parts orders must contain Model Number, Parts Number and Description.
2. Ordering quantity of resistors, capacitors and screws must be multiple of 10pcs.
3. Component parts indicated by parentheses in the column Q'ty are not available.

PARTS LIST

Schematic Location	Parts No.	Description	Q'ty
or		SI TR 2SC1941	1
Q601		SI TR 2SC536	1
or		SI TR 2SC945	1
Q602		SI TR 2SD400	1
Q603		SI TR 2SD823	1
or		SI TR 2SC2373	1
Q604		SI TR 2SC536	1
or		SI TR 2SC945	1
Q701		SI TR 2SD613	1
Q702		SI TR 2SC536	1
or		SI TR 2SC945	1
Q703		SI TR 2SC536	1
or		SI TR 2SC945	1
V901		CRT 240YB4	1
or		CRT 240XB4A	1

SANYO ELECTRIC INC.
1200, WEST ARTESIA BLVD.
P.O. BOX 5177
COMPTON, CALIFORNIA 90220
Feb. 1980 CP1000 Printed in Japan

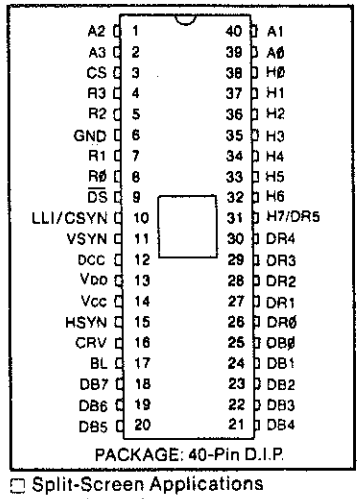
CRT 5027
CRT 5037
CRT 5057*
μPC FAMILY

CRT Video Timer-Controller
VTAC®

FEATURES

- ☐ Fully Programmable Display Format
  - Characters per data row (1-200)
  - Data rows per frame (1-64)
  - Raster scans per data row (1-16)
- ☐ Programmable Monitor Sync Format
  - Raster Scans/Frame (256-1023)
  - "Front Porch"
  - Sync Width
  - "Back Porch"
  - Interlace/Non-Interlace
  - Vertical Blanking
- ☐ Lock Line Input (CRT 5057)
- ☐ Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync (CRT 5027, CRT 5037)
  - Blanking
  - Cursor coincidence
- ☐ Programmed via:
  - Processor data bus
  - External PROM
  - Mask Option ROM
- ☐ Standard or Non-Standard CRT Monitor Compatible
- ☐ Refresh Rate: 60Hz, 50Hz,...
- ☐ Scrolling
  - Single Line
  - Multi-Line
- ☐ Cursor Position Registers
- ☐ Character Format: 5x7, 7x9,...
- ☐ Programmable Vertical Data Positioning
- ☐ Balanced Beam Current Interlace (CRT 5037)
- ☐ Graphics Compatible

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

- ☐ Split-Screen Applications
  - Horizontal
  - Vertical
- ☐ Interlace or Non-Interlace operation
- ☐ TTL Compatibility
- ☐ BUS Oriented
- ☐ High Speed Operation
- ☐ COPLAMOS® N-Channel Silicon Gate Technology
- ☐ Compatible with CRT 8002 VDAC™
- ☐ Compatible with CRT 7004

GENERAL DESCRIPTION

The CRT Video Timer-Controller Chip (VTAC)® is a user programmable 40-pin COPLAMOS®n channel MOS/LSI device containing the logic functions required to generate all the timing signals for the presentation and formatting of interlaced and non-interlaced video data on a standard or non-standard CRT monitor.

With the exception of the dot counter, which may be clocked at a video frequency above 25 MHz and therefore not recommended for MOS implementation, all frame formatting, such as horizontal, vertical, and composite sync, characters per data row, data rows per frame, and raster scans per data row and per frame are totally user programmable. The data row counter has been designed to facilitate scrolling.

Programming is effected by loading seven 8 bit control registers directly off an 8 bit bidirectional data bus. Four register address lines and a chip select line provide complete microprocessor compatibility for program controlled set up. The device can be "self loaded" via an external PROM tied on the data bus as described in the OPERATION section. Formatting can also be programmed by a single mask option.

In addition to the seven control registers two additional registers are provided to store the cursor character and data row addresses for generation of the cursor video signal. The contents of these two registers can also be read out onto the bus for update by the program.

Three versions of the VTAC® are available. The CRT 5027 provides non-interlaced operation with an even or odd number of scan lines per data row, or interlaced operation with an even number of scan lines per data row. The CRT 5037 may be programmed for an odd or even number of scan lines per data row in both interlaced and non-interlaced modes. Programming the CRT 5037 for an odd number of scan lines per data row eliminates character distortion caused by the uneven beam current normally associated with odd field/even field interlacing of alphanumeric displays.

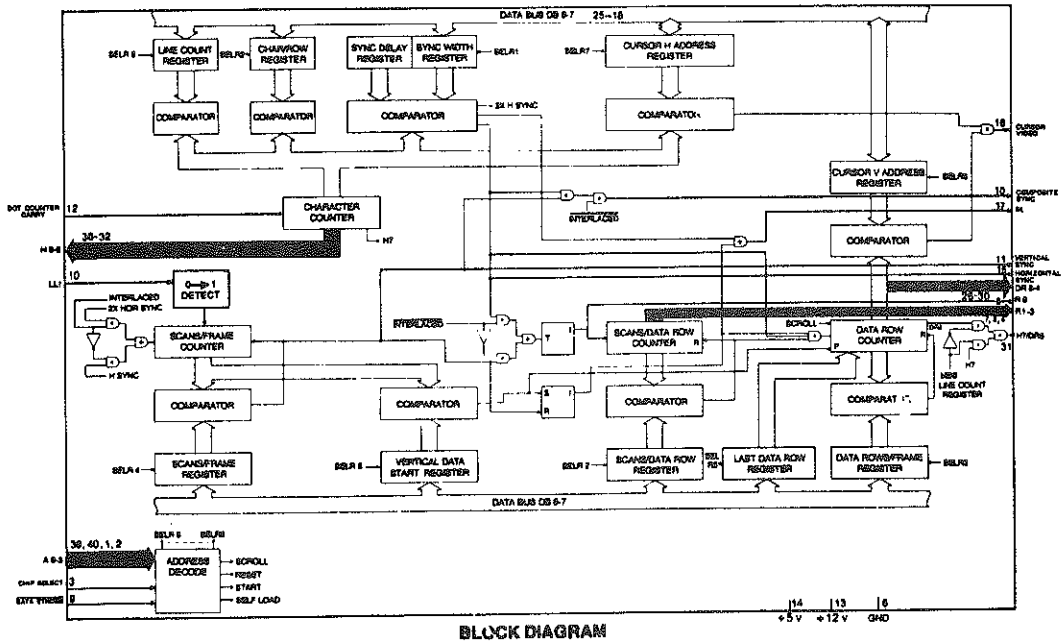
The CRT 5057 provides the ability to lock a CRT's vertical refresh rate, as controlled by the VTAC's® vertical sync pulse, to the 50 Hz or 60 Hz line frequency thereby eliminating the so called "swim" phenomenon. This is particularly well suited for European system requirements. The line frequency waveform, processed to conform to the VTAC's® specified logic levels, is applied to the line lock input. The VTAC® will inhibit generation of vertical sync until a zero to one transition on this input is detected. The vertical sync pulse is then initiated within one scan line after this transition rises above the logic threshold of the VTAC.®

To provide the pin required for the line lock input, the composite sync output is not provided in the CRT 5057.

*FOR FUTURE RELEASE

Description of Pin Functions

Pin No.	Symbol	Name	Input/ Output	Function
25-18	DBØ-7	Data Bus	I/O	Data bus. Input bus for control words from microprocessor or PROM. Bidirectional bus for cursor address.
3	CS	Chip Select	I	Signals chip that it is being addressed
39, 40, 1, 2	AØ-3	Register Address	I	Register address bits for selecting one of seven control registers or either of the cursor address registers
9	$\overline{DS}$	Data Strobe	I	Strobes DBØ-7 into the appropriate register or outputs the cursor character address or cursor line address onto the data bus
12	DCC	DOT Counter Carry	I	Carry from off chip dot counter establishing basic character clock rate. Character clock.
38-32	HØ-6	Character Counter Outputs	O	Character counter outputs.
7, 5, 4	R1-3	Scan Counter Outputs	O	Three most significant bits of the Scan Counter; row select inputs to character generator.
31	H7/DR5	H7/DR5	O	Pin definition is user programmable. Output is MSB of Character Counter if horizontal line count (REG.Ø) is ≥128; otherwise output is MSB of Data Row Counter.
8	RØ	Scan Counter LSB	O	Least significant bit of the scan counter. In the interlaced mode with an even number of scans per data row, RØ will toggle at the field rate; for an odd number of scans per data row in the interlaced mode, RØ will toggle at the data row rate.
26-30	DRØ-4	Data Row Counter Outputs	O	Data Row counter outputs.
17	BL	Blank	O	Defines non active portion of horizontal and vertical scans.
15	HSYN	Horizontal Sync	O	Initiates horizontal retrace.
11	VSYN	Vertical Sync	O	Initiates vertical retrace.
10	CSYN/ LLI	Composite Sync Output/ Line Lock Input	O/I	Composite sync is provided on the CRT 5027 and CRT 5037. This output is active in non-interlaced mode only. Provides a true RS-170 composite sync wave form. For the CRT 5057, this pin is the Line Lock Input. The line frequency waveform, processed to conform to the VTAC's® specified logic levels, is applied to this pin.
16	CRV	Cursor Video	O	Defines cursor location in data field.
14	Vcc	Power Supply	PS	+5 volt Power Supply
13	VDD	Power Supply	PS	+12 volt Power Supply



BLOCK DIAGRAM

8251A
PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous and Asynchronous Operation**
- **Synchronous 5-8 Bit Characters; Internal or External Character Synchronization; Automatic Sync Insertion**
- **Asynchronous 5-8 Bit Characters; Clock Rate—1, 16 or 64 Times Baud Rate; Break Character Generation; 1, 1½, or 2 Stop Bits; False Start Bit Detection; Automatic Break Detect and Handling**
- **Synchronous Baud Rate—DC to 64K Baud**
- **Asynchronous Baud Rate—DC to 19.2K Baud**
- **Full-Duplex, Double-Buffered Transmitter and Receiver**
- **Error Detection—Parity, Overrun and Framing**
- **Compatible with an Extended Range of Intel Microprocessors**
- **28-Pin DIP Package**
- **All Inputs and Outputs are TTL Compatible**
- **Single +5V Supply**
- **Single TTL Clock**

The Intel® 8251A is the enhanced version of the industry standard, Intel 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Intel's microprocessor families such as MCS-48, 80, 85, and iAPX-86, 88. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is fabricated using N-channel silicon gate technology.

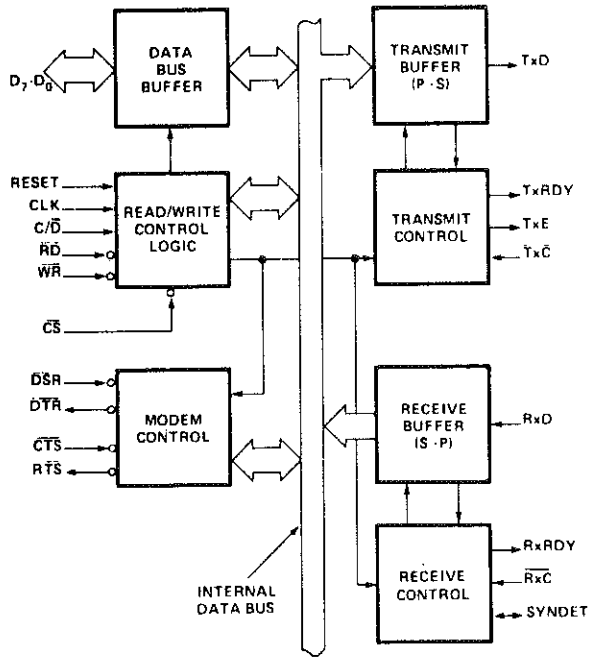


Figure 1. Block Diagram

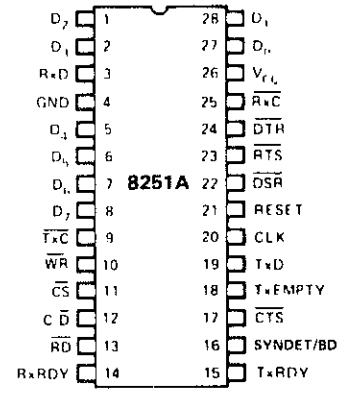


Figure 2. Pin Configuration

FEATURES AND ENHANCEMENTS

The 8251A is an advanced design of the industry standard USART, the Intel® 8251. The 8251A operates with an extended range of Intel microprocessors and maintains compatibility with the 8251. Familiarization time is minimal because of compatibility and involves only knowing the additional features and enhancements, and reviewing the AC and DC specifications of the 8251A.

The 8251A incorporates all the key features of the 8251 and has the following additional features and enhancements:

- 8251A has double-buffered data paths with separate I/O registers for control, status, Data In, and Data Out, which considerably simplifies control programming and minimizes CPU overhead.
- In asynchronous operations, the Receiver detects and handles "break" automatically, relieving the CPU of this task.
- A refined Rx initialization prevents the Receiver from starting when in "break" state, preventing unwanted interrupts from a disconnected USART.
- At the conclusion of a transmission, TxD line will always return to the marking state unless SBRK is programmed.
- Tx Enable logic enhancement prevents a Tx Disable command from halting transmission until all data previously written has been transmitted. The logic also prevents the transmitter from turning off in the middle of a word.
- When External Sync Detect is programmed, Internal Sync Detect is disabled, and an External Sync Detect status is provided via a flip-flop which clears itself upon a status read.
- Possibility of false sync detect is minimized by ensuring that if double character sync is programmed, the characters be contiguously detected and also by clearing the Rx register to all ones whenever Enter Hunt command is issued in Sync mode.
- As long as the 8251A is not selected, the $\overline{RD}$ and $\overline{WR}$ do not affect the internal operation of the device.
- The 8251A Status can be read at any time but the status update will be inhibited during status read.
- The 8251A is free from extraneous glitches and has enhanced AC and DC characteristics, providing higher speed and better operating margins.
- Synchronous Baud rate from DC to 64K.

FUNCTIONAL DESCRIPTION

General

The 8251A is a Universal Synchronous/Asynchronous Receiver/Transmitter designed for a wide range of Intel microcomputers such as 8048, 8080, 8085, 8086 and 8088. Like other I/O devices in a microcomputer system, its functional configuration is programmed by the system's software for maximum flexibility. The 8251A can support most serial data techniques in use, including IBM "bi-sync."

In a communication environment an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear "transparent" to the CPU, a simple input or output of byte-oriented system data.

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the 8251A to the system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the CPU. Control words, Command words and Status information are also transferred through the Data Bus Buffer. The Command Status, Data-In and Data-Out registers are separate, 8-bit registers communicating with the system bus through the Data Bus Buffer.

This functional block accepts inputs from the system Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for the device functional definition.

RESET (Reset)

A "high" on this input forces the 8251A into an "Idle" mode. The device will remain at "Idle" until a new set of control words is written into the 8251A to program its functional definition. Minimum RESET pulse width is 6 t_{CY} (clock must be running).

A command reset operation also puts the device into the "Idle" state.

Z80® CPU Central Processing Unit

Zilog

Product Specification

Features

- The instruction set contains 158 instructions. The 78 instructions of the 8080A are included as a subset; 8080A software compatibility is maintained.
- Six MHz, 4 MHz and 2.5 MHz clocks for the Z80B, Z80A, and Z80 CPU result in rapid instruction execution with consequent high data throughput.
- The extensive instruction set includes string, bit, byte, and word operations. Block searches and block transfers together with indexed and relative addressing result in the most powerful data handling capabilities in the microcomputer industry.
- The Z80 microprocessors and associated family of peripheral controllers are linked by a vectored interrupt system. This system may be daisy-chained to allow implementation of a priority interrupt scheme. Little, if any, additional logic is required for daisy-chaining.
- Duplicate sets of both general-purpose and flag registers are provided, easing the design and operation of system software through single-context switching, background-foreground programming, and single-level interrupt processing. In addition, two 16-bit index registers facilitate program processing of tables and arrays.
- There are three modes of high speed interrupt processing: 8080 compatible, non-Z80 peripheral device, and Z80 Family peripheral with or without daisy chain.
- On-chip dynamic memory refresh counter.

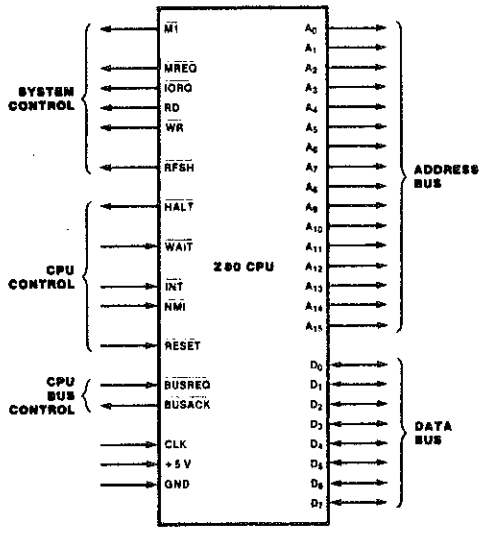


Figure 1. Pin Functions

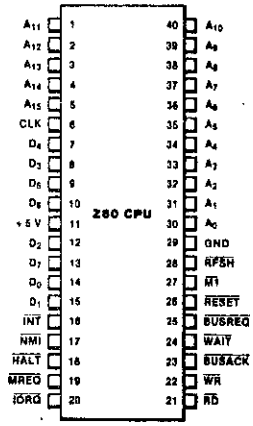


Figure 2. Pin Assignments

General Description

The Z80, Z80A, and Z80B CPUs are third-generation single-chip microprocessors with exceptional computational power. They offer higher system throughput and more efficient memory utilization than comparable second- and third-generation microprocessors. The internal registers contain 208 bits of read/write memory that are accessible to the programmer. These registers include two sets of six general-purpose registers which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition, there are two sets of accumulator and flag registers. A group of "Exchange" instructions makes either set of main or alternate registers accessible to the programmer. The alternate set allows operation in foreground-background mode or it may be reserved for very fast interrupt response.

The Z80 also contains a Stack Pointer, Program Counter, two index registers, a Refresh register (counter), and an Interrupt register. The CPU is easy to incorporate into a system since it requires only a single +5 V power source, all output signals are fully decoded and timed to control standard memory or peripheral circuits, and is supported by an extensive family of peripheral controllers. The internal block diagram (Figure 3) shows the primary functions of the Z80 processors. Subsequent text provides more detail on the Z80 I/O controller family, registers, instruction set, interrupts and daisy chaining, and CPU timing.

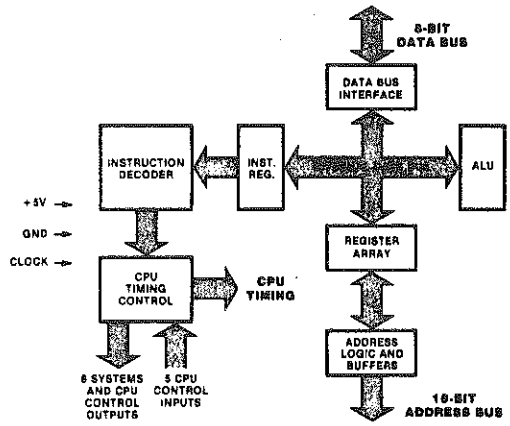


Figure 3. Z80 CPU Block Diagram

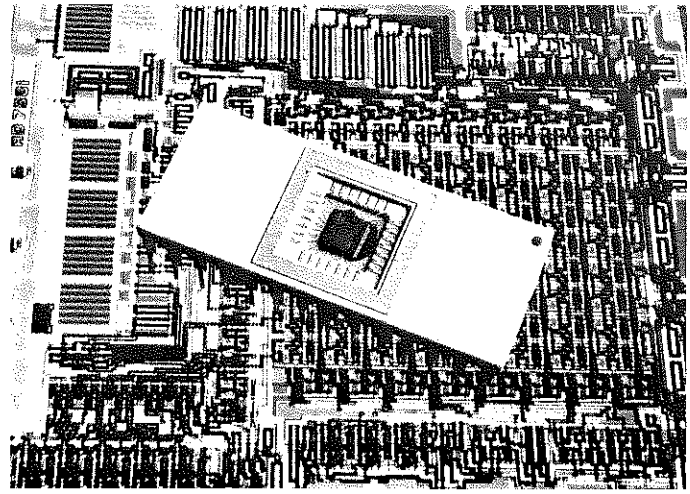
ANALOG DEVICES

CMOS µP Compatible 8-Bit 8-Channel DAS

AD7581

FEATURES

- 8-Bit Resolution
- On-Chip 8 X 8 Dual-Port Memory
- No Missed Codes Over Full Temperature Range
- Interfaces Directly to Z80/8085/6800
- CMOS, TTL Compatible Digital Inputs
- Three-State Data Drivers
- Ratiometric Capability
- Single +5V Supply
- Interleaved DMA Operation
- Fast Conversion
- A/D Process Totally Transparent to µP
- Low Cost

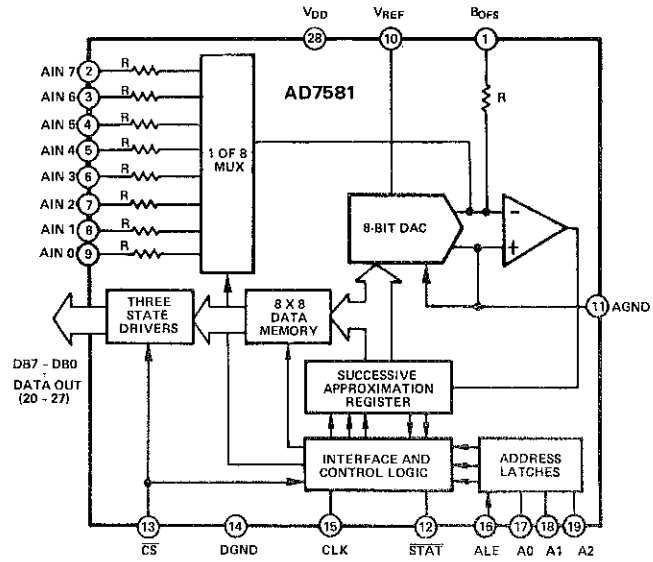


GENERAL DESCRIPTION

The AD7581 is a microprocessor compatible 8 bit, 8 channel, memory buffered, data-acquisition system on a monolithic CMOS chip. It consists of an 8 bit successive approximation A/D converter, an 8 channel multiplexer, 8 X 8 dual-port RAM, three-state DATA drivers (for interface), address latches and microprocessor compatible control logic. The device interfaces directly to 8080, 8085, Z80, 6800 and other microprocessor systems.

The successive approximation conversion takes place on a continuous, channel sequencing, basis using microprocessor control signals for the clock. Data is automatically transferred to its proper location in the 8 X 8 dual-port RAM at the end of each conversion. When under microprocessor control, a READ DATA operation is allowed at any time for any channel since on-chip logic provides interleaved DMA. The facility to latch the address inputs ($A_0 - A_2$) with ALE enables the AD7581 to interface with µP systems which feature either shared or separate address and data buses.

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

Differential Nonlinearity	Temperature Range and Package: Plastic 0 to +70°C	Temperature Range and Package: Ceramic -25°C to +85°C
±1 7/8LSB	AD7581JN	AD7581AD
±7/8LSB	AD7581KN	AD7581BD
±3/4LSB	AD7581LN	AD7581CD

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast 714/842-1717 Mid-West 312/894-3300 Texas 214/231-5094

DC SPECIFICATIONS (V_{DD} = +5V, V_{REF} = -10V, Unipolar Operation, unless otherwise stated)

Parameter	Version[1]	Typical at +25°C	Limit Over Temperature	Units	Conditions/Comments
ACCURACY					
Resolution	All	8	8	Bits	
Relative Accuracy	JN, AD	±1 7/8	±1 7/8 max	LSB	
	KN, BD	±3/4	±3/4 max	LSB	
	LN, CD	±1/2	±1/2 max	LSB	
Differential Nonlinearity	JN, AD	±1 7/8	±1 7/8 max	LSB	
	KN, BD	±7/8	±7/8 max	LSB	
	LN, CD	±3/4	±3/4 max	LSB	
Offset Error[2]	JN, AD	200	200 max	mV	Adjustable to zero, see Figure 7a.
	KN, BD	80	80 max	mV	
	LN, CD	50	50 max	mV	
Gain Error					
Worst Channel	JN, AD	±3	±6 max	LSB	Adjustable to zero, see Figure 7a.
	KN, BD	±2	±4 max	LSB	Gain Error is Measured After Offset
	LN, CD	±1	±2 max	LSB	Calibration. Max Full Scale Change for Any Channel from +25°C to T_{min} or T_{max} is ±2LSB.
Gain Match Between Channels	JN, AD	2	3 max	LSB	Adjustable to zero, see Figure 7a.
	KN, BD	1 1/2	2 max	LSB	
	LN, CD	1	1 max	LSB	
B_{OFS} Gain Error	All	-2 1/2	—	LSB	
ANALOG INPUTS					
Input Resistance					
At V_{REF} (pin 10)	All	10/20/30	10/20/30	kΩ min/typ/max	
At B_{OFS} (pin 1)[3]	All	10/20/30	10/20/30	kΩ min/typ/max	
At Any Analog Input (pins 2-9)	All	10/20/30	10/20/30	kΩ min/typ/max	
V_{REF} (For Specified Performance)	All	-10	-10	V	±5%
V_{REF} Range[4]	All	-5 to -15	-5 to -15	V	
Nominal Analog Input Range					
Unipolar Mode	All	0 to $+V_{REF}$, 0 to $-V_{REF}$	0 to $+V_{REF}$ 0 to $-V_{REF}$	V V	See Figure 7 and 8.
Bipolar Mode	All	$-VB_{OFS} \leq VA_{IN} \leq \lvert V_{REF} \rvert - VB_{OFS}$			See Figure 9
DIGITAL INPUTS					
$\overline{CS}$ (pin 13), ALE (pin 16), A_0 - A_2 (pins 17-19)					
CLK (pin 15)					
V_{INH} Logic HIGH Input Voltage	All	+2.2	+2.4 min	V	
V_{INL} Logic LOW Input Voltage	All	+0.4	+0.8 max	V	
I_{IN} Input Current	All	0.01	1 max	μA	V_{IN} = 0V, V_{DD}
C_{IN} Input Capacitance[5]	All	4	5 max	pF	
DIGITAL OUTPUTS					
$\overline{STAT}$ (pin 12), DB_7 to DB_0 (pins 20-27)					
V_{OH} Output HIGH Voltage	All	+4.8	+4.5 min	V	I_{SOURCE} = 40μA
V_{OL} Output LOW Voltage	All	+0.4	+0.6 max	V	I_{SINK} = 1.6mA
I_{LKG} DB_7 to DB_0 Floating State Leakage	All	0.3	10 max	μA	
Floating State Output Capacitance (DB_7 - DB_0)	All	5	10 max	pF	V_{OUT} = 0V to V_{DD}
Output Code	All	Unipolar Binary Figure 7 Complementary Binary Figure 8 Offset Binary Figure 9			
POWER REQUIREMENTS					
V_{DD}	All	+5	+5	V	
I_{DD} - Static	All	3 typ	5 max	mA	
I_{DD} - Dynamic	All	3 typ	8 max	mA	f_{CLK} = 1MHz

Notes:
[1] Temperature range as follows: JN, KN, LN (0 to +70°C), AD, BD, CD (-25°C to +85°C).
[2] Typical offset temperature coefficient is ±150μV/°C.
[3] R_{BOFS}/R_{AIN} (0-7) mismatch causes transfer function rotation about positive full scale. The effect is an offset and a gain term when using the circuits of Figure 8a, page 6 and Figure 9a, page 7.
[4] Typical value, not guaranteed or subject to test.
[5] Guaranteed but not tested.
[6] Typical change in B_{OFS} gain from +25°C to T_{min} to T_{max} is ±2 LSB's.

Specifications subject to change without notice.

MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MC146818

Advance Information

CMOS

(HIGH-PERFORMANCE
SILICON-GATE COMPLEMENTARY MOS)

REAL-TIME CLOCK
PLUS RAM

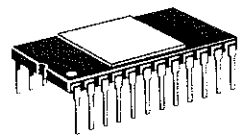
REAL-TIME CLOCK PLUS RAM (RTC)

The MC146818 Real-Time Clock plus RAM is a peripheral device which includes the unique MOTEL concept for use with various microprocessors, microcomputers, and larger computers. This part combines three unique features: a complete time-of-day clock with alarm and one hundred year calendar, a programmable periodic interrupt and square-wave generator, and 50 bytes of low-power static RAM. The MC146818 uses high-speed CMOS technology to interface with 1 MHz processor buses, while consuming very little power.

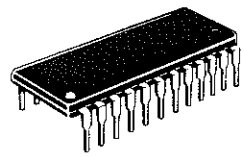
The Real-Time Clock plus RAM has two distinct uses. First, it is designed as a battery powered CMOS part (in an otherwise NMOS/TTL system) including all the common battery backed-up functions such as RAM, time, and calendar. Secondly, the MC146818 may be used with a CMOS microprocessor to relieve the software of the timekeeping workload and to extend the available RAM of an MPU such as the MC146805E2.

- Low-Power, High-Speed, High-Density CMOS
- Internal Time Base and Oscillator
- Counts Seconds, Minutes, and Hours of the Day
- Counts Days of the Week, Date, Month, and Year
- 3 V to 6 V Operation
- Time Base Input Options: 4.194304 MHz, 1.048576 MHz, or 32.768 kHz
- Time Base Oscillator for Parallel Resonant Crystals
- 40 to 200 μW Typical Operating Power at Low Frequency Time Base
- 4.0 to 20 mW Typical Operating Power at High Frequency Time Base
- Binary or BCD Representation of Time, Calendar, and Alarm
- 12- or 24-Hour Clock with AM and PM in 12-Hour Mode
- Daylight Savings Time Option
- Automatic End of Month Recognition
- Automatic Leap Year Compensation
- Microprocessor Bus Compatible
- MOTEL Circuit for Bus Universality
- Multiplexed Bus for Pin Efficiency
- Interfaced with Software as 64 RAM Locations
- 14 Bytes of Clock and Control Registers
- 50 Bytes of General Purpose RAM
- Status Bit Indicates Data Integrity
- Bus Compatible Interrupt Signals ($\overline{IRQ}$)
- Three Interrupts are Separately Software Maskable and Testable
  - Time-of-Day Alarm, Once-per-Second to Once-per-Day
  - Periodic Rates from 30.5 μs to 500 ms
  - End-of-Clock Update Cycle
- Programmable Square-Wave Output Signal
- Clock Output May Be Used as Microprocessor Clock Input
  - At Time Base Frequency ÷1 or ÷4
- 24-Pin Dual-In-Line Package
- Chip Carrier Also Available

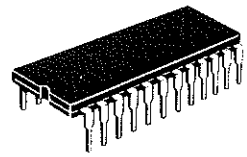
L SUFFIX
CERAMIC PACKAGE
CASE 716



P SUFFIX
PLASTIC PACKAGE
CASE 709

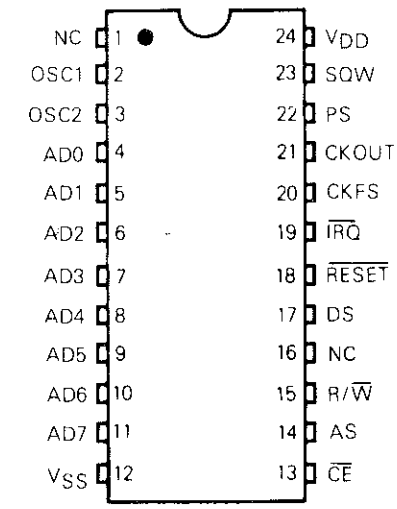


S SUFFIX
CERDIP PACKAGE
CASE 623



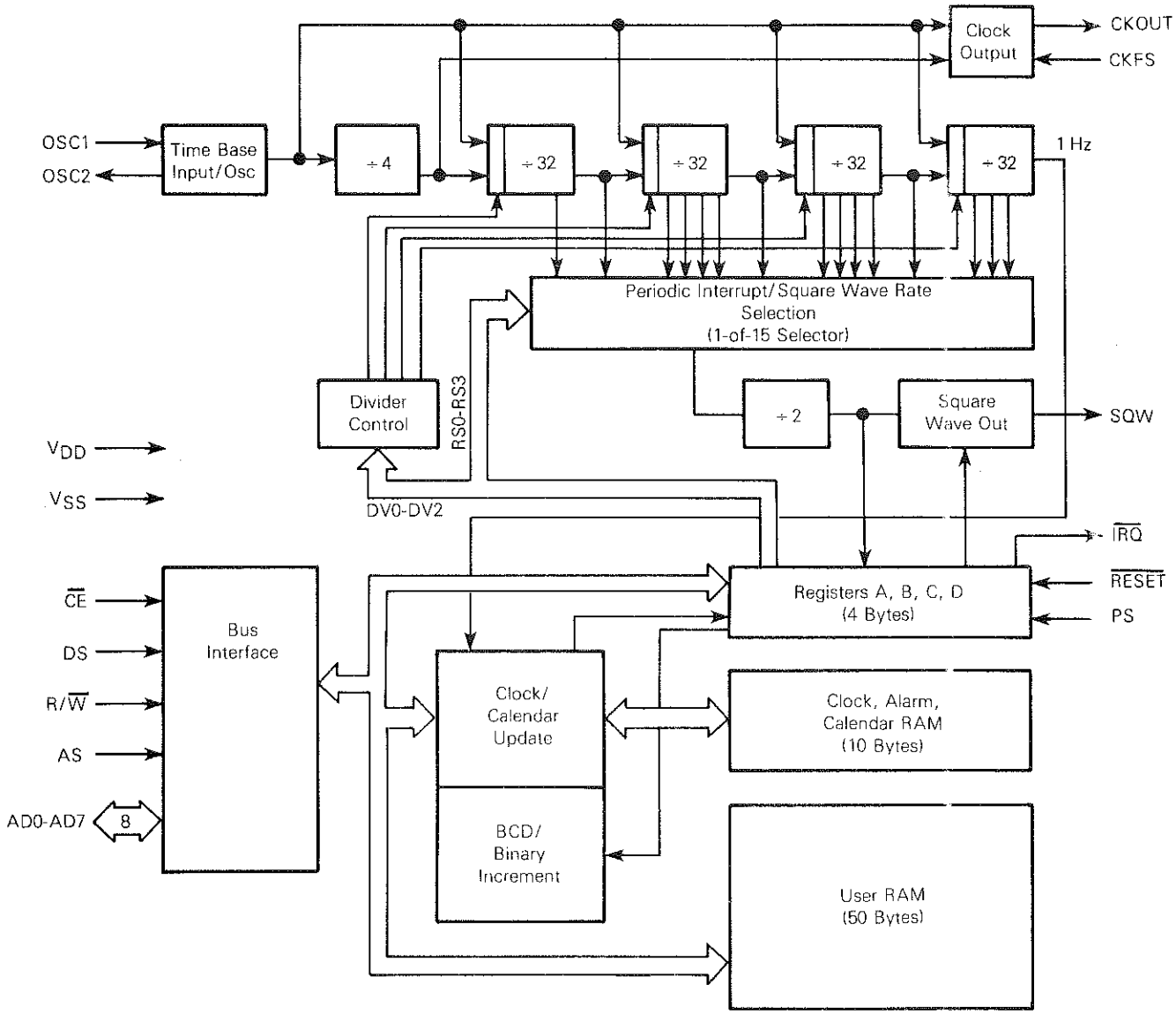
CHIP CARRIER
ALSO AVAILABLE

PIN ASSIGNMENTS



This document contains information on a new product. Specifications and information herein are subject to change without notice.

FIGURE 1 — BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 to +8.0	V
All Input Voltages Except OSC1	V_{in}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
Current Drain per Pin Excluding V_{DD} and V_{SS}	I	10	mA
Operating Temperature Range MC146818 MC146818C (V_{DD} = 3.0 to 5.5 V operation)	T_A	T_L to T_H 0 to 70 −40 to 85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic Cerdip Ceramic	θ_{JA}	 120 65 50	°C/W

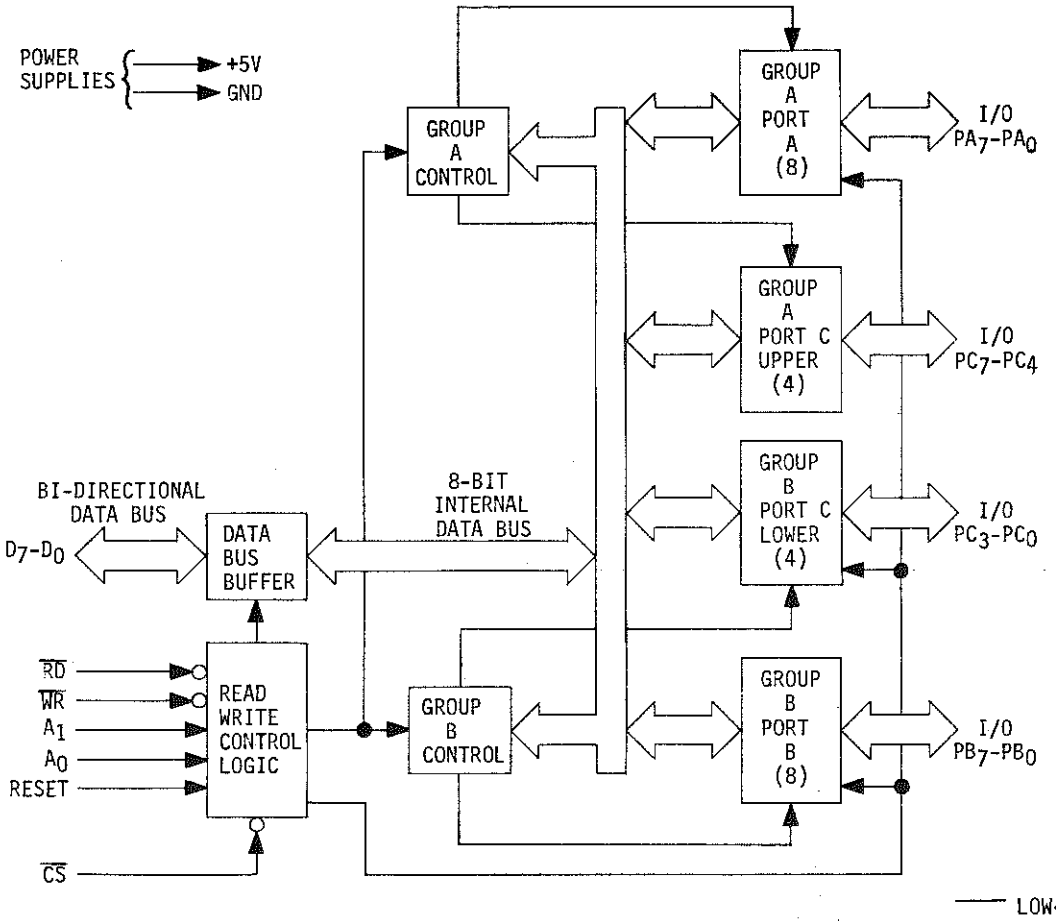


FIGURE 1. 8255A BLOCK DIAGRAM

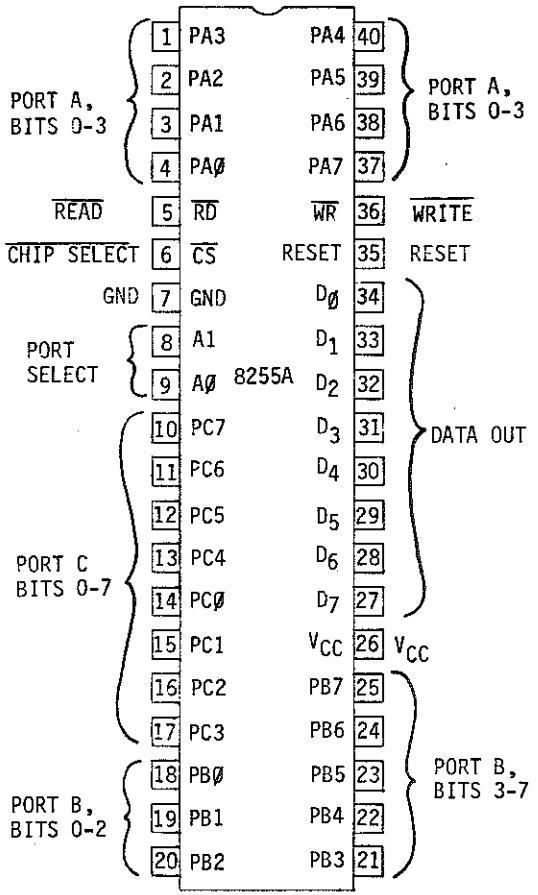


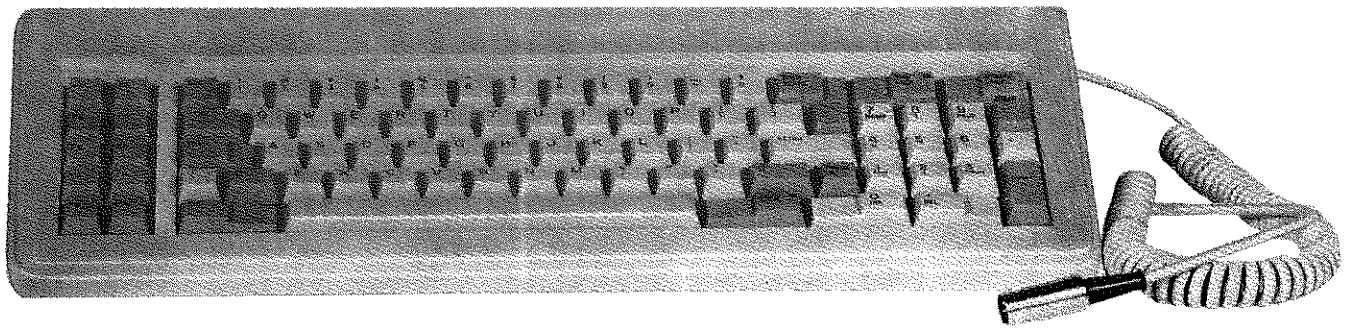
FIGURE 2. PIN CONFIGURATION

The Intel 8255A is a general purpose programmable I/O device designed for use with Intel microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

597-0036-30

Low Profile — Silent - Tactile Capacitance Keyboard

84ST13-1E



Personal Computer Compatible Keyboard (Serial ASCII Interface With Enhanced Key Array)

FEATURES

- IBM personal computer compatible key array with serial ASCII interface
- Standard listing includes DIN compatible enclosure and data interface cable
- Meets European ergonomic standards
- Operator preferred silent-tactile feel
- Solid state capacitance switching
- Status LEDs for Caps Lock and Numeric Lock keys
- Multiple interface options
- Diagnostic self-test after power-up or reset
- Multi-key rollover
- 8 character FIFO buffer
- Sculptured double shot molded keytops

MICRO SWITCH 84ST13-1E features an enhanced IBM personal computer key array with serial ASCII interface. The keyboard with enclosure and a 6 foot (extended length) coiled cord provides complete final package requirements for detached keyboard assemblies. The high strength injection molded plastic enclosure has a cloud white matte finish. Other colors can be provided. The keyboard combines capacitance-membrane switching with a microcomputer and custom detector circuit to provide solid state reliability with increased functionality.

The 84ST13-1E features a low profile design that allows customers to meet European ergonomic standards. These standards state the keyboard (mounted in an enclosure) must be no more than 30 mm (1.18") when measured from the middle of the home row to the table top.

All ST Series keyboards are UL recognized and CSA certified.

MICROCOMPUTER

The keyboard uses a scanning system where each key is individually tested for its state (operated or non-operated). Scanning and detection is accomplished by a custom 28 pin (LSI) IC capacitance detector in conjunction with a microcomputer. The custom detector uses 9 active drive lines and 11 active sense lines which interface with the capacitance-membrane key matrix. (Refer to Keyboard Schematic, page 7). In addition to the power supply lines, there is a clock, key output and reset line that interfaces with the microcomputer. The microcomputer includes an 8-bit CPU, a ROM, RAM, I/O lines and a timer/event counter.

HUMAN FACTORS ORIENTED

Every aspect of this keyboard is designed for maximum operator throughput. This includes a low profile design, proven operating force displacement characteristics, key spacing, keytop shapes, double-shot molded sculptured keytops, block array and a touch typing key arrangement. Actuating key modules are designed to provide silent operation and positive tactile feedback without trade-off. Tactile feedback is felt by the operator as an abrupt change in force at the operating point of the module. Silent operation allows quieter office environments regardless of the number of terminals. Multi-key rollover and a 8 character FIFO (first-in first-out) buffer is included for high throughput. A 10 ±1 Hertz repeat rate is available on all keys. Status LEDs on Caps Lock and Num Lock tell at a glance which modes these keys are in greatly reducing chance entry of false data or command.

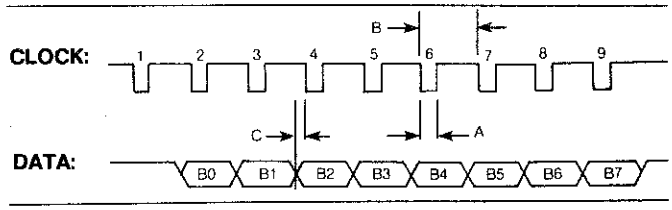
Personal Computer Keyboard

ELECTRICAL DATA

Note: The keyboard panel must be electrically connected to system chassis ground to prevent electrostatic damage and noise pickup.

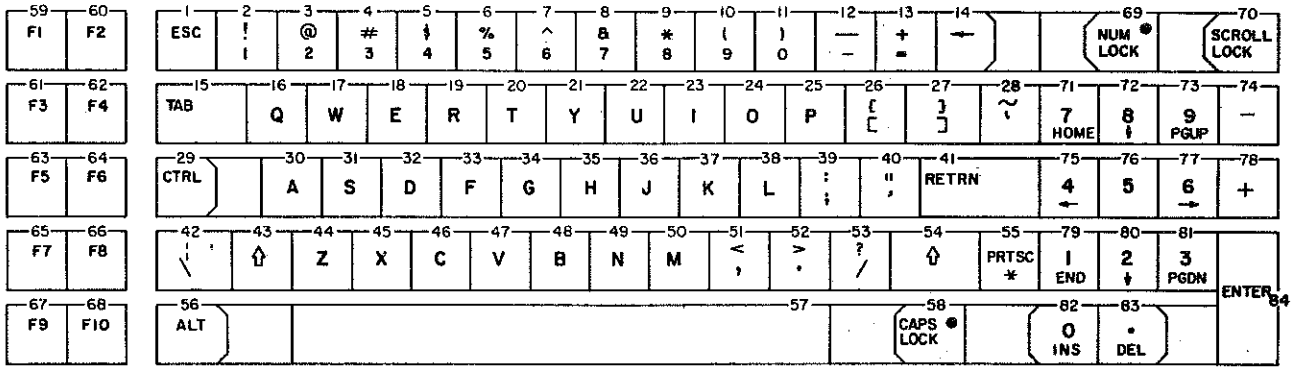
Power Requirements	+5 VDC ±5% @ 300 mA (max.)
Input/Output Specifications	Data transmission is differential TTL. Both keyboard positive data (+Data) and keyboard negative data (-Data) is 9600 ±2% Baud. Each keyboard +Data transmission consists of 1 start bit (low level), 8 data bits (positive logic) odd parity and 2 stop bits (high level). Each keyboard -Data transmission consists of 1 start bit (high level), 8 data bits (negative logic) odd parity and 2 stop bits (low level).
	Output Logic Logic "0"; 0.4 VDC max. @ 12 mA max. (sinking). Logic "1"; 2.4 VDC min. @ 600 μA max. (sourcing).
	Input Logic (Inhibit Only) Logic "0"; 0.4 VDC max. @ 4.5 mA max. (sinking). Logic "1"; 2.4 VDC min. @ 600 μA max. (leakage).
Auto Repeat	All keys with the exception of the Mode keys (stations 29, 42, 54, 56, 58 and 69) will auto repeat. A key will start to auto repeat once it is depressed and held down for a period of 500 ±20% milliseconds. The keyboard will then repeat at a rate of 10 ±2 Hertz.
Keystroke Buffer	An 8-character FIFO (first-in, first-out) keystroke buffer is provided. If the FIFO buffer overflows, additional keystrokes will be ignored until space is available in the buffer.
Inhibit	The output of the keyboard can be inhibited by taking the +Data line to Logic "0". The FIFO buffer will store keycodes while the keyboard is inhibited. The keyboard checks the +Data line prior to transmission. The keyboard ignores inhibit during transmission.
LED Operation (Caps Lock and Num Lock)	First depression of the key turns On the LED. The second depression turns Off the LED. LEDs are Off on Power-up and software Reset. Caps Lock Key (58), when operated, puts the following keys into shift mode when they are operated: 16 thru 25, 30 thru 38 and 44 thru 50. Num Lock Key (69), when operated puts the following keys into shift mode when they are operated: 71 thru 73, 75 thru 77, and 79 thru 83.
ALT Mode	When the ALT key (key 56) is depressed bit 8 (most significant bit) of the data transmission is cleared.

ELECTRICAL DATA FOR OPTIONAL IBM INTERFACE (With J15 out and J16 installed)

Power Requirements	+5 VDC $^{+6\%}_{-0}$ @ 300 mA (max.)
Input/Output Specifications (Synchronous Operation J5 Out and J6 In)	The keyboard will check the status of the "Clock" line and the "Data" line prior to every data transmission. If either line is low, then no keyboard transmission is allowed. If both lines are high, then the keyboard will initiate transmission by leaving the "Data" line High and clocking the start bit to the host system on the falling edge of the clock pulse. The keyboard will then clock the eight data bits to the host system on the falling edge of each clock pulse. The keyboard will raise the "Data" line within one clock period after the ninth clock pulse to complete the transmission. The keyboard will not check the status of either line during data transmission.  Baud = 25,000 A = 10 μsecs. $\pm$ 1 μsec. B = 40 μsecs. $\pm$ 2% C = 1.0 μsecs minimum. 1. Reset Line (Not Used) 2. Data Line + Keyboard Data - Busy Each keyboard transmission on the "Data" line consists of 1 start bit (high level) and 8 data bits (positive logic, "LSB" sent first) Logic "1"; 2.4 VDC min @ 600 μA max sourcing (keyboard output) 2.4 VDC min @ 600 μA max leakage (keyboard input) Logic "0"; 0.4 VDC max @ 12 mA max sinking (keyboard output) 0.4 VDC max @ 4.5 mA sinking (keyboard input) 3. "Clock" Line + Keyboard Clock-Reset (software) Logic "1"; 2.4 VDC min @ 600 μA max sourcing (keyboard output) 2.4 VDC min @ 600 μA max leakage (keyboard input) Logic "0"; 0.4 VDC max @ 12 mA max sinking (keyboard output) 0.4 VDC max @ 4.5 mA sinking (keyboard input)
Key Operation	All keys are Make/Break and repeatable. The most significant bit of each scan code is a low level for key depressions and a high level for key releases. When a key is depressed, the keyboard will transmit its assigned scan code. If the key is held depressed for a period of 500 milliseconds $\pm$ 50 milliseconds, its assigned scan code will be transmitted at a 10 Hz. $\pm$ 1 Hz. repeat rate for as long as the key is held depressed or until another key is operated. Depression of a second key will cause the first key to stop repeating and the scan code of the second key to be transmitted, as well as initiation of a delay sequence.
LED Operation (Caps Lock and Num Lock)	First depression of the key turns On the LED. The second depression turns Off the LED. LEDs are Off on Power-up and software Reset.
Keystroke Buffer	A 15-character (First-in, First-out) keystroke buffer is provided to prevent loss of keystrokes. An "FF HEX" Code will be inserted into the buffer, overlaying the last data byte entered. If the keystroke overflows, the keyboard will transmit this code once it has reached the top of the buffer.
Keyboard Diagnosis	The keyboard microprocessor will perform a diagnostic self-test after Power-Up or after the host system signals the keyboard to perform a software reset by toggling the Clock line low for 500 microseconds minimum. The microprocessor will check its data memory locations, do a sum-check on its program memory and check for any depressed keys. If the diagnostic test is correct, the keyboard will transmit an "AA HEX" Code. This will be the first transmission following a Power-Up condition. If the diagnostic test was unsuccessful, then the keyboard will transmit an "80HEX" Code. In either case, after the keyboard diagnostic check the keyboard will begin normal operation.

Personal Computer Keyboard

CHARACTER ARRAY ASSIGNMENTS

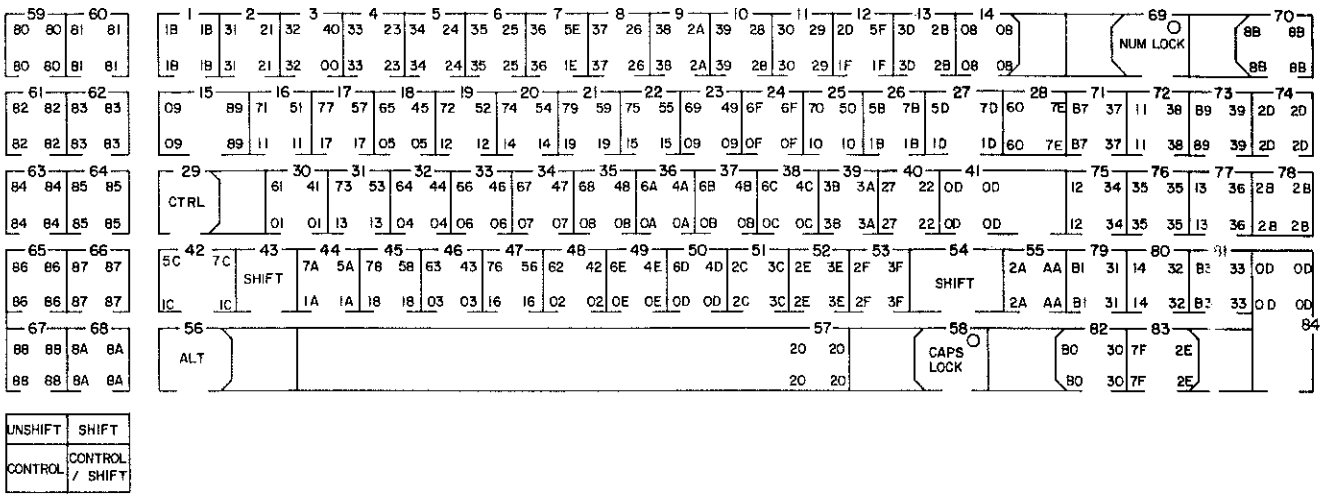


KEYTOPS
The 84ST13-1E array features double shot molded sculptured keytops. The right and left block array keytops are medium gray (1-57) shells with dark gray (1-49) legends. The touch typing keytops are light gray (1-58) shells with dark gray (1-49) legends. Keystation 70 has a black ink front stamp legend. All keytops are matte finish. The LEDs in keystation 58 and 69 are red.

KEYBOARD STYLE
Stepped with a 3/8-3/16-3/8 offset between rows within the staggered array. Keys are spaced on 3/4 inch center.

TERMINATION
Amp 87576-1 or equivalent (right angle header).

USASCII CODE ASSIGNMENT (standard)



In ALT mode bit 7 is cleared for +Data and set for -Data.

USASCII HEX-CODE ASSIGNMENT

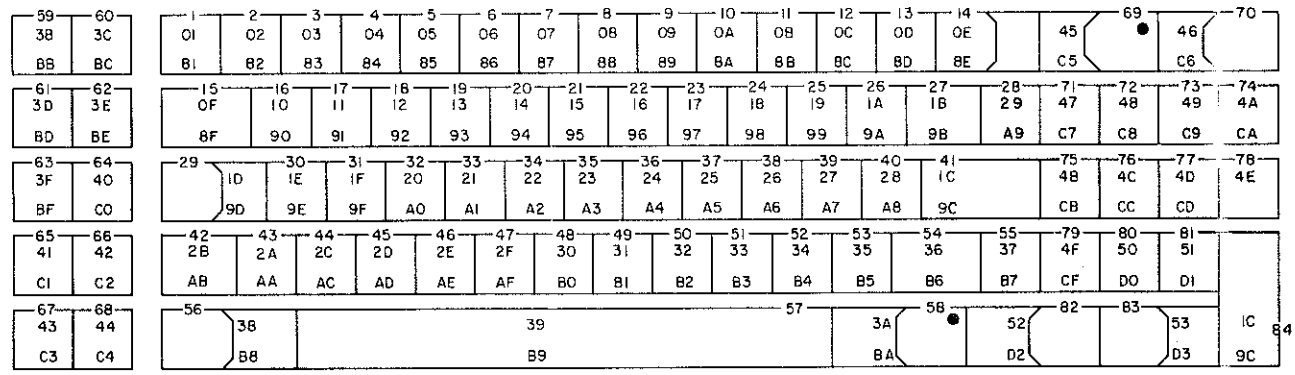
The 84ST13-1E is furnished encoded with the 8-bit USASCII code plus odd parity. There are four modes of operation: Unshift, Shift, Control and Control/Shift. Refer to page 4 for the Character Assignments and above for the Code Assignments.

The bit assignments for each key are shown in the hexadecimal numbering system. Hexadecimal means 16 and is simply a shorthand notation used to express the binary bit patterns. This system uses binary bits to count up to 16, carry, and then start counting again. It does not, however, count to 16 in numbers. It counts from 0 through 9 in numbers; then 10 is A, 11 is B, 12 is C, 13 is D, 14 is E and 15 is F.

Since the 84ST13-1E uses eight bits for each character, each byte can be thought of as being two hexadecimal system digits. The example below shows the binary code assignment of key #50 (m) in all four modes of operations.

	Unshift	
Hexadecimal	6	D
Binary	0110	1101
	Shift	
Hexadecimal	4	D
Binary	0100	1101
	Control	
Hexadecimal	0	D
Binary	0000	1101
	Control/Shift	
Hexadecimal	0	D
Binary	0000	1101

8-BIT IBM CODE ASSIGNMENT (Optional)



All keycodes are in hexadecimal

8-BIT IBM HEX-CODE ASSIGNMENT

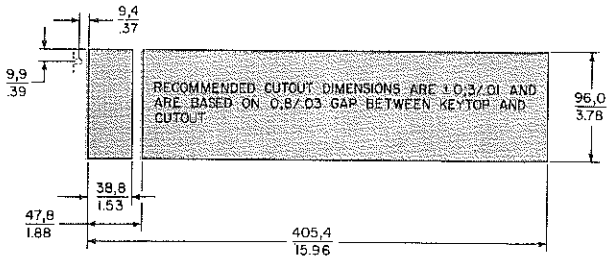
Remove J15 and install J16 to obtain the IBM Code Set.

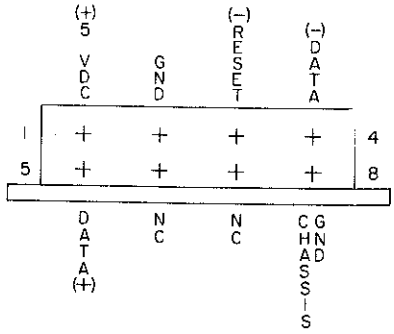
The keys shown in the IBM code chart will output a 8-bit code for a depression (make) or a release (break) and are electrical compatible with the IBM personal computer keyboard. Refer to page 4 for the key characters.

Personal Computer Keyboard

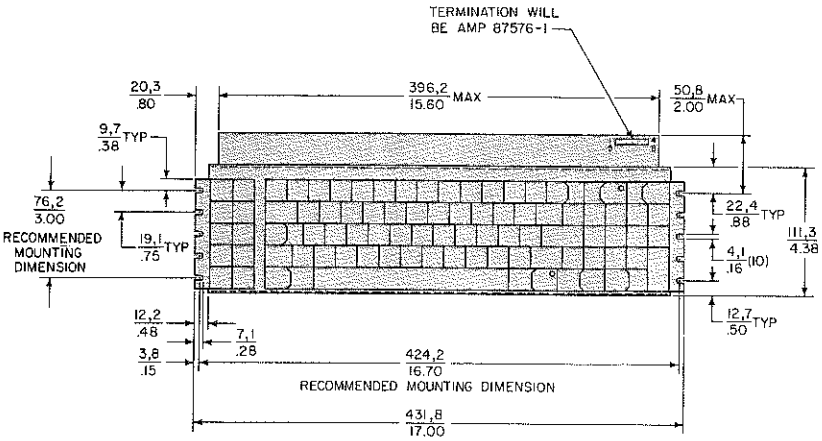
MOUNTING DIMENSIONS
(For reference only)

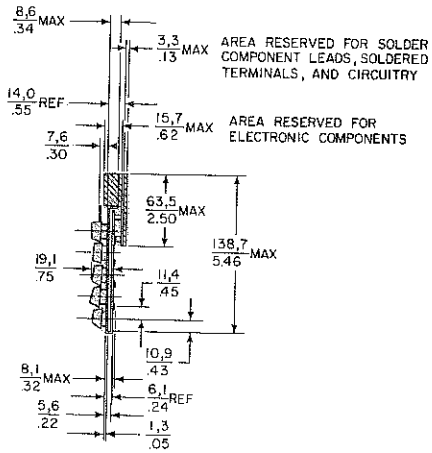
0,0 mm
0.00 inches



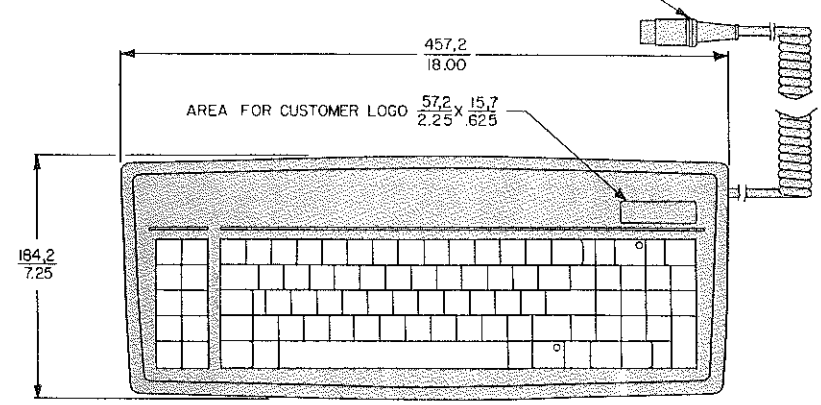


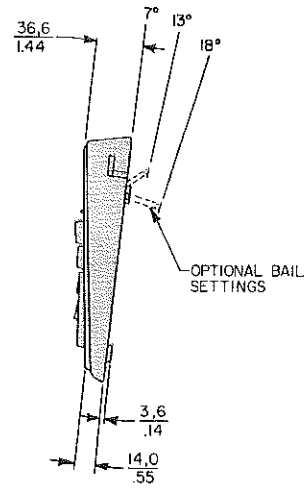
TERMINATION
Amp 8576-1 or equivalent (right angle header).





CABLE ASSEMBLY - 5 PIN MALE AUDIO DIN PLUG, 180° ARRANGEMENT, EACH PIN AT 45°; 5 CONDUCTOR PLUS SHIELD (#26 AWG MIN), 6' COILED COIL (PRACTICAL EXTENDED LENGTH); CABLE JACKET COLOR-DRIFTWOOD.





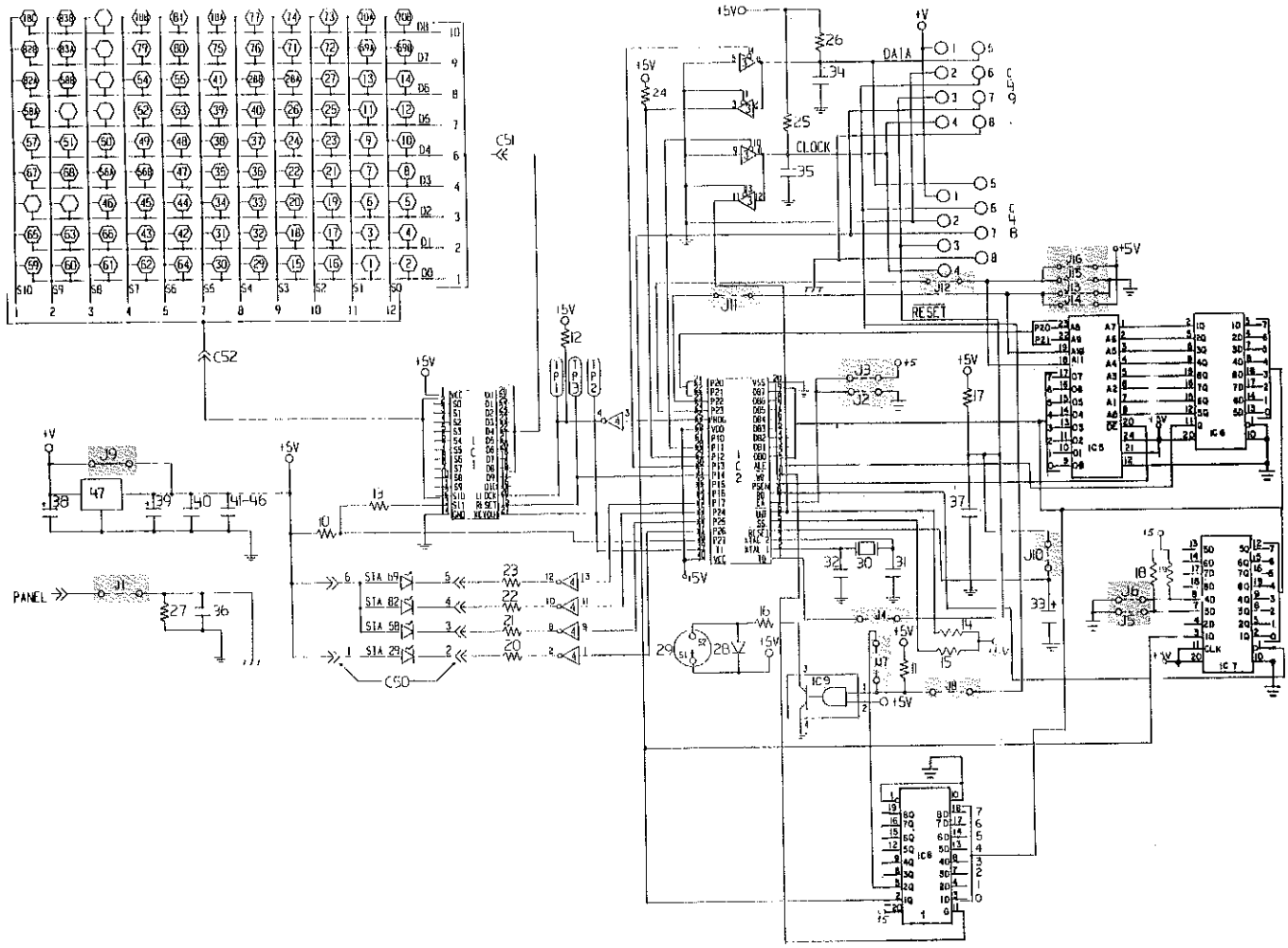
CONNECTOR TERMINATION
(SWITCHCRAFT 05GM5M OR EQUIVALENT).

SWITCHCRAFT 05GM5M OR EQUIVALENT

Pin	Signal
5	+5 VDC
4	Ground
3	Reset (Not Connected)
1	-Data*
2	+Data
Shell	Chassis Ground

*Synchronous clock line when IBM interface is selected.

KEYBOARD SCHEMATIC



- Supply +5.0 ±0.25 VDC (voltage regulator not installed) measured at connector terminals.
- IC packs contain +5 VDC on pin 14 and ground on pin 7 unless otherwise noted.
- Do not make connections to unidentified termination pads.
- Shaded area indicates jumper connections.

KEYBOARD OPTIONS

Additional flexibility has been engineered into the keyboard. With the addition or removal of a wire jumper the following options become available:

Baud Rates	J5	J6		
	Out	Out	9600	
	Out	In	SYNC - IBM	
	In	Out	1200	
	In	In	300	
USASCII or IBM	J12	J15	J16	
Codes	Out	In	Out	USASCII Standard)
	Out	Out	In	IBM Compatible
Voltage Regulator	12 VDC ±10% @ 300 mA max.			
Audio Feedback Circuit	2048 ±5% Hertz for 2.75 ±5% miliseconds software controlled. Activated by first depressing and holding down stations 29, 42, 56, 58 and 54 respectively. Deactivated by second depression. Audio feedback deactivates after Power-up reset.			

Personal Computer Keyboard

84ST13-1E

SALES AND SERVICE
MICRO SWITCH field engineers in sales offices throughout the United States, Canada and Europe are ready to work with you in satisfying your keyboard requirements: proper selection, pricing and delivery scheduling. These keyboard experts will provide sound and practical answers to your needs.

UNITED STATES
MICRO SWITCH
A Honeywell Division
Chicago & Spring Sts.
Freeport, IL 61032
Tel. 815/235-6600

CANADA
Honeywell Limited
The Honeywell Centre
155 Gordon Baker Rd.
Willowdale, Ontario
M2H 3N7.
Tel. 416/499-6111

EUROPE
Honeywell Europe S.A.
MICRO SWITCH Division
Av. Henri Matisse 14
1140 Brussels, Belgium
Telephone (02) 243-1211

Together, we can find the answers.

MICRO SWITCH
a Honeywell Division

84-07537-0 785 Printed in USA

PRODUCT WARRANTY

LIMITED ONE YEAR

While this warranty gives you specific legal rights, which terminate one (1) year (6 months on turntable motors) from the date of shipment, you may also have other rights which vary from state to state.

Broadcast Electronics, Inc. ("BE"), 4100 North 24th Street, P. O. Box 3606, Quincy, Illinois 62305, hereby warrants cartridge machines, consoles, transmitters and other new Equipment manufactured by BE against any defects in material or workmanship at the time of delivery thereof, that develop under normal use within a period of one (1) year (6 months for turntable motors) from the date of shipment. Other manufacturers' Equipment, if any, shall carry only such manufacturers' standard warranty. This warranty extends to the original user and any subsequent purchaser during the warranty period. BE's sole responsibility with respect to any Equipment or parts not conforming to this warranty is to replace such equipment or parts upon the return thereof F.O.B. BE's factory or authorized repair depot within the period aforesaid.

In the event of replacement pursuant to the foregoing warranty, only the unexpired portion of the warranty from the time of the original purchase will remain in effect for any such replacement. However, the warranty period will be extended for the length of time that the original user is without the services of the Equipment due to its being serviced pursuant to this warranty. The terms of the foregoing warranty shall be null and void if the Equipment has been altered or repaired without specific written authorization of BE, or if Equipment is operated under environmental conditions or circumstances other than those specifically described in BE's product literature or instruction manual which accompany the Equipment purchased. BE shall not be liable for any expense of any nature whatsoever incurred by the original user without prior written consent of BE.

BE shall not be liable to the original user for any and all incidental or consequential damages for breach of either expressed or implied warranties. However, some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation or exclusion may not apply to you. All express and implied warranties shall terminate at the conclusion of the period set forth herein.

Except as set forth herein, and except as to title, there are no warranties, or any affirmations of fact or promises by BE, with reference to the Equipment, or to merchantability, fitness for a particular application, signal coverage, infringement, or otherwise, which extend beyond the description of the Equipment in BE's product literature or instruction manual which accompany the Equipment. Any card which is enclosed with the Equipment will be used by BE for survey purposes only.

BROADCAST ELECTRONICS, INC.
4100 North 24th Street, P. O. Box 3606, Quincy, Illinois 62305